# Spartan-3 Starter Kit Board User Guide

UG130 (v1.0) April 26, 2004

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# Spartan-3 Starter Kit Board User Guide
# UG130 (v1.0) April 26, 2004

The following table shows the revision history for this document..

| | Version | Revision |
|---|---|---|
| 04/26/04 | 1.0 | Initial Xilinx release. |

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# About This Guide

This user guide describes the components and operation of the Spartan-3 Starter Kit Board.

## Guide Contents

This manual contains the following chapters:

- Chapter 1, “Introduction”
- Chapter 2, “Fast, Asynchronous SRAM”
- Chapter 3, “Four-Digit, Seven-Segment LED Display”
- Chapter 4, “Switches and LEDs”
- Chapter 5, “VGA Port”
- Chapter 6, “PS/2 Mouse/Keyboard Port”
- Chapter 7, “RS-232 Port”
- Chapter 8, “Clock Sources”
- Chapter 9, “FPGA Configuration Modes and Functions”
- Chapter 10, “Platform Flash Configuration Storage”
- Chapter 11, “JTAG Programming/Debugging Ports”
- Chapter 12, “Power Distribution”
- Appendix A, “Board Schematics”
- Appendix B, “Reference Material for Major Components”

## Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

| Resource | Description/URL |
|---|---|
| Tutorials | Tutorials covering Xilinx design flows, from design entry to verification and debugging<br>http://support.xilinx.com/support/techsup/tutorials/index.htm |
| Answer Browser | Database of Xilinx solution records<br>http://support.xilinx.com/xlnx/xil_ans_browser.jsp |

| Resource | Description/URL |
|---|---|
| Application Notes | Descriptions of device-specific design techniques and approaches<br>http://support.xilinx.com/apps/appsweb.htm |
| Data Sheets | Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging<br>http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp |
| Problem Solvers | Interactive tools that allow you to troubleshoot your design issues<br>http://support.xilinx.com/support/troubleshoot/psolvers.htm |
| Tech Tips | Latest news, design tips, and patch information for the Xilinx design environment<br>http://www.support.xilinx.com/xlnx/xil_tt_home.jsp |

# Conventions

This document uses the following conventions. An example illustrates each convention.

## Typographical

The following typographical conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| `Courier font` | Messages, prompts, and program files that the system displays | `speed grade: - 100` |
| **`Courier bold`** | Literal commands that you enter in a syntactical statement | **`ngdbuild`** *`design_name`* |
| **Helvetica bold** | Commands that you select from a menu | **File →Open** |
| | Keyboard shortcuts | **Ctrl+C** |
| *Italic font* | Variables in a syntax statement for which you must supply values | **`ngdbuild`** *`design_name`* |
| | References to other manuals | See the *Development System Reference Guide* for more information. |
| | Emphasis in text | If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected. |
| Square brackets [ ] | An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required. | **`ngdbuild`** `[`*`option_name`*`]` *`design_name`* |

| Convention | Meaning or Use | Example |
|---|---|---|
| Braces { } | A list of items from which you must choose one or more | `lowpwr ={on\|off}` |
| Vertical bar \| | Separates items in a list of choices | `lowpwr ={on\|off}` |
| Vertical ellipsis<br>.<br>.<br>. | Repetitive material that has been omitted | `IOB #1: Name = QOUT'`<br>`IOB #2: Name = CLKIN'`<br>.<br>.<br>. |
| Horizontal ellipsis ... | Repetitive material that has been omitted | `allow block block_name loc1 loc2 ... locn;` |

## Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---|---|---|
| Blue text | Cross-reference link to a location in the current document | See the section "Additional Resources" for details.<br>Refer to "Title Formats" in Chapter 1 for details. |
| Red text | Cross-reference link to a location in another document | See Figure 2-5 in the *Virtex-II Handbook*. |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest speed files. |

Chapter 1

# Introduction

The Xilinx Spartan-3 Starter Kit provides a low-cost, easy-to-use development and evaluation platform for Spartan-3 FPGA designs.

## Key Components and Features

Figure 1-1 shows the Spartan-3 Starter Kit board, which includes the following components and features:

- 200,000-gate Xilinx Spartan-3 XC3S200 FPGA in a 256-ball thin Ball Grid Array package (XC3S200FT256) (1)
  - 4,320 logic cell equivalents
  - Twelve 18K-bit block RAMs (216K bits)
  - Twelve 18x18 hardware multipliers
  - Four Digital Clock Managers (DCMs)
  - Up to 173 user-defined I/O signals
- 2Mbit Xilinx XCF02S Platform Flash, in-system programmable configuration PROM (2)
  - 1Mbit non-volatile data or application code storage available after FPGA configuration
  - Jumper options allow FPGA application to read PROM data or FPGA configuration from other sources (3)
- 1M-byte of Fast Asynchronous SRAM (bottom side of board, see Figure 1-3) (4)
  - Two 256Kx16 ISSI IS61LV25616AL-10T 10 ns SRAMs
  - Configurable memory architecture
    - Single 256Kx32 SRAM array, ideal for MicroBlaze code images
    - Two independent 256Kx16 SRAM arrays
  - Individual chip select per device
  - Individual byte enables
- 3-bit, 8-color VGA display port (5)
- 9-pin RS-232 Serial Port (6)
  - DB9 9-pin female connector (DCE connector)
  - Maxim MAX3232 RS-232 transceiver/translator (7)
  - Uses straight-through serial cable to connect to computer or workstation serial port
  - Second RS-232 transmit and receive channel available on board test points (8)

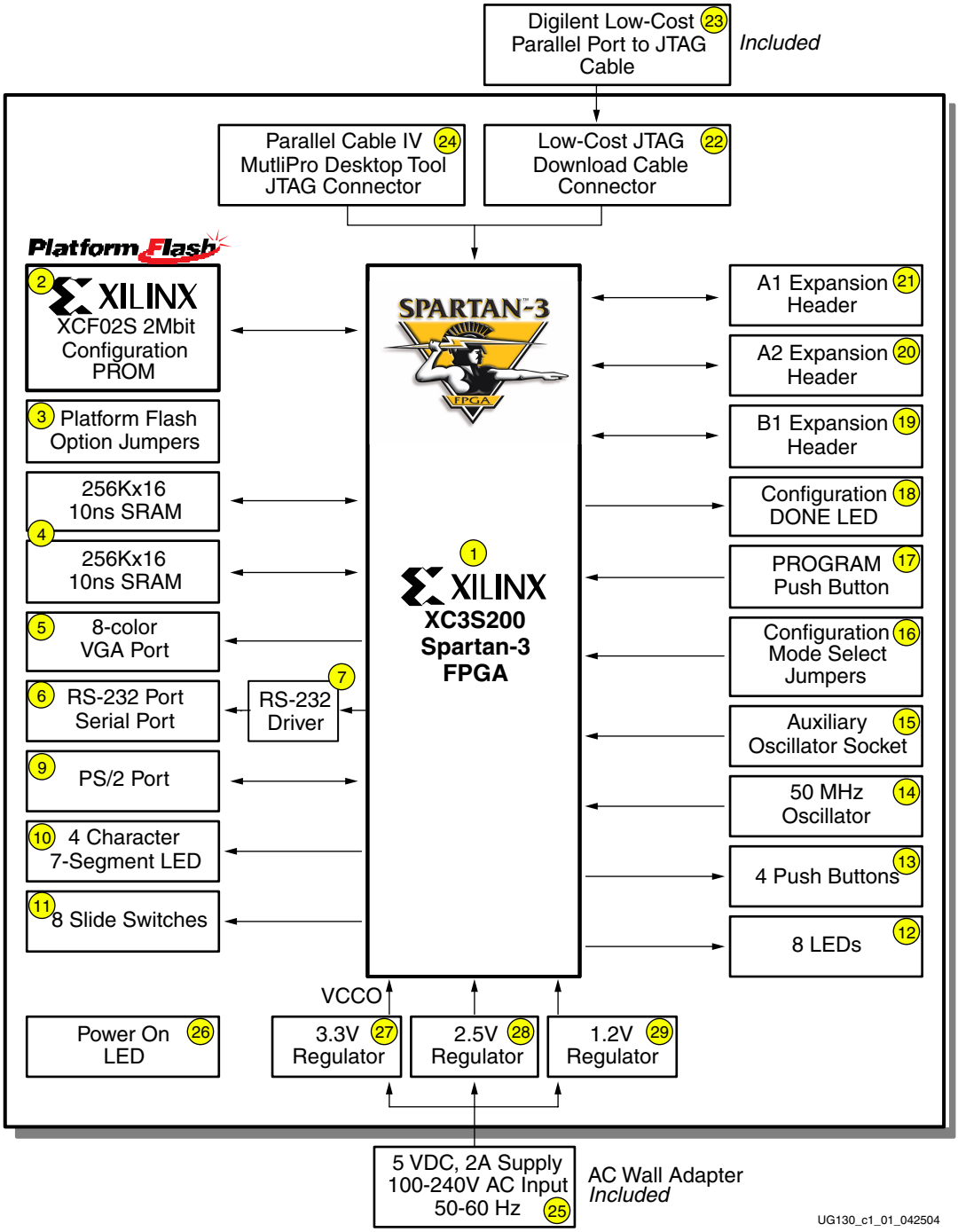



*Figure 1-1:* **Xilinx Spartan-3 Starter Kit Board Block Diagram**

- PS/2-style mouse/keyboard port (9)
- Four-character, seven-segment LED display (10)
- Eight slide switches (11)
- Eight individual LED outputs (12)
- Four momentary-contact push button switches (13)

- 50 MHz crystal oscillator clock source (bottom side of board, see Figure 1-3) (14)
- Socket for an auxiliary crystal oscillator clock source (15)
- FPGA configuration mode selected via jumper settings (16)
- Push button switch to force FPGA reconfiguration (FPGA configuration happens automatically at power-on) (17)
- LED indicates when FPGA is successfully configured (18)
- Three 40-pin expansion connection ports to extend and enhance the Spartan-3 Starter Kit Board (19) (20) (21)
  - See www.xilinx.com/s3board for compatible expansion cards
  - Compatible with Digilent, Inc. peripheral boards https://digilent.us/Sales/boards.cfm#Peripheral
  - FPGA serial configuration interface signals available on the A2 and B1 connectors
    - PROG_B, DONE, INIT_B, CCLK, DONE
- JTAG port (22) for low-cost download cable (23)
- Digilent JTAG download/debugging cable connects to PC parallel port (23)
- JTAG download/debug port compatible with the Xilinx Parallel Cable IV and MultiPRO Desktop Tool (24)
- AC power adapter input for included international unregulated +5V power supply (25)
- Power-on indicator LED (26)
- On-board 3.3V (27), 2.5V (28), and 1.2V (29) regulators

# Component Locations

Figure 1-2 and Figure 1-3 indicate the component locations on the top side and bottom side of the board, respectively.

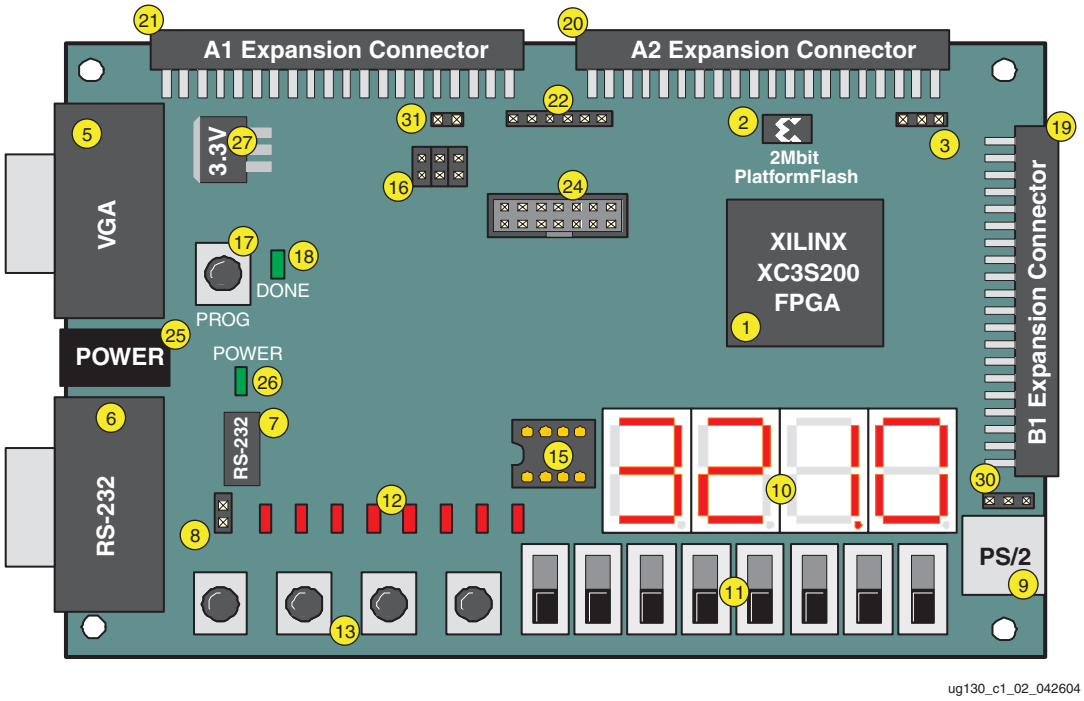



*Figure 1-2:* **Xilinx Spartan-3 Starter Kit Board (Top Side)**

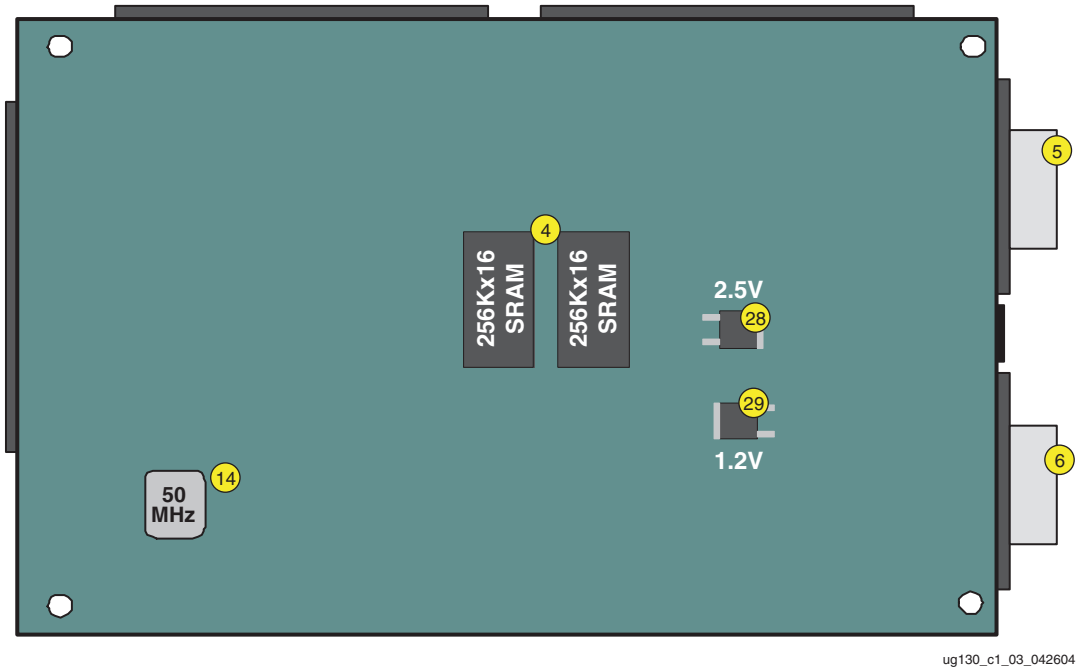



*Figure 1-3:* **Xilinx Spartan-3 Starter Kit Board (Bottom Side)**

Chapter 2

# Fast, Asynchronous SRAM

The Spartan-3 Starter Kit board has a megabyte of fast asynchronous SRAM, surface-mounted to the backside of the board. The memory array includes two 256Kx16 ISSI IS61LV25616AL-10T 10 ns SRAM devices, as shown in Figure 2-1. A detailed schematic appears in Figure A-8.

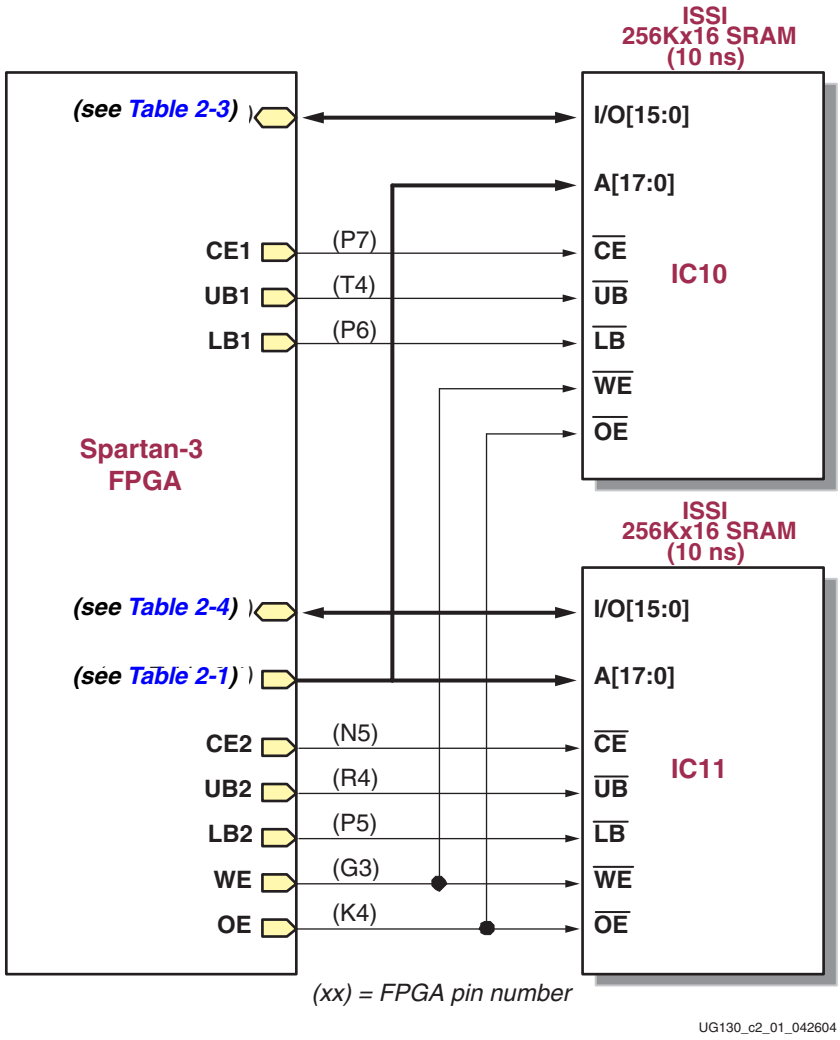



*Figure 2-1:* **FPGA to SRAM Connections**

The SRAM array forms either a single 256Kx32 SRAM memory or two independent 256Kx16 arrays. Both SRAM devices share common write-enable (WE#), output-enable (OE#), and address (A[17:0]) signals. However, each device has a separate chip select (CS#) control and individual byte-enable controls to select the high or low byte in the 16-bit data word, UB and LB, respectively.

The 256Kx32 configuration is ideally suited to hold MicroBlaze instructions. However, it alternately provides high-density data storage for a variety of applications, such as digital signal processing (DSP), large data FIFOs, and graphics buffers.

## Address Bus Connections

Both 256Kx16 SRAMs share 18-bit address control lines, as shown in Table 2-1. These address signals also connect to the A1 Expansion Connector (see "Expansion Connectors," page 51).

*Table 2-1:* **External SRAM Address Bus Connections to Spartan-3 FPGA**

| Address Bit | FPGA Pin | A1 Expansion Connector Pin |
|---|---|---|
| A17 | L3 | 35 |
| A16 | K5 | 33 |
| A15 | K3 | 34 |
| A14 | J3 | 31 |
| A13 | J4 | 32 |
| A12 | H4 | 29 |
| A11 | H3 | 30 |
| A10 | G5 | 27 |
| A9 | E4 | 28 |
| A8 | E3 | 25 |
| A7 | F4 | 26 |
| A6 | F3 | 23 |
| A5 | G4 | 24 |
| A4 | L4 | 14 |
| A3 | M3 | 12 |
| A2 | M4 | 10 |
| A1 | N3 | 8 |
| A0 | L5 | 6 |

# Write Enable and Output Enable Control Signals

Both 256Kx16 SRAMs share common output enable (OE#) and write enable (WE#) control lines, as shown in Table 2-2. These control signals also connect to the A1 Expansion Connector (refer to "Expansion Connectors," page 51).

*Table 2-2:* **External SRAM Control Signal Connections to Spartan-3 FPGA**

| Signal | FPGA Pin | A1 Expansion Connector Pin |
|---|---|---|
| OE# | K4 | 16 |
| WE# | G3 | 18 |

# SRAM Data Signals, Chip Enables, and Byte Enables

The data signals, chip enables, and byte enables are dedicated connections between the FPGA and SRAM. Table 2-3 shows the FPGA pin connections to the SRAM designated IC10 in Figure A-8. Table 2-4 shows the FPGA pin connections to SRAM IC11.

*Table 2-3:* **SRAM IC10 Connections**

| Signal | FPGA Pin |
|---|---|
| IO15 | R1 |
| IO14 | P1 |
| IO13 | L2 |
| IO12 | J2 |
| IO11 | H1 |
| IO10 | F2 |
| IO9 | P8 |
| IO8 | D3 |
| IO7 | B1 |
| IO6 | C1 |
| IO5 | C2 |
| IO4 | R5 |
| IO3 | T5 |
| IO2 | R6 |
| IO1 | T8 |
| IO0 | N7 |
| CE1 (chip enable IC10) | P7 |
| UB1 (upper byte enable IC10) | T4 |
| LB1 (lower byte enable IC10) | P6 |

*Table 2-4:* **SRAM IC11 Connections**

| Signal | FPGA Pin |
|---|---|
| IO15 | N1 |
| IO14 | M1 |
| IO13 | K2 |
| IO12 | C3 |
| IO11 | F5 |
| IO10 | G1 |
| IO9 | E2 |
| IO8 | D2 |
| IO7 | D1 |
| IO6 | E1 |
| IO5 | G2 |
| IO4 | J1 |
| IO3 | K1 |
| IO2 | M2 |
| IO1 | N2 |
| IO0 | P2 |
| CE2 (chip enable IC11) | N5 |
| UB2 (upper byte enable IC11) | R4 |
| LB2 (lower byte enable IC11) | P5 |

To disable an SRAM, drive the associated chip enable pin High.

Chapter 3

# Four-Digit, Seven-Segment LED Display

The Spartan-3 Starter Kit board has a four-character, seven segment LED display controlled by FPGA user-I/O pins, as shown in Figure 3-1. Each digit shares eight common control signals to light individual LED segments. Each individual character has a separate anode control input. A detailed schematic for the display appears in Figure A-2.

The pin number for each FPGA pin connected to the LED display appears in parentheses. To light an individual signal, drive the individual segment control signal Low along with the associated anode control signal for the individual character. In Figure 3-1, for example, the left-most character displays the value '2'. The digital values driving the display in this example are shown in blue. The AN3 anode control signal is Low, enabling the control inputs for the left-most character. The segment control inputs, A through G and DP, drive the individual segments that comprise the character. A Low value lights the individual segment, a High turns off the segment. A Low on the A input signal, lights segment 'a' of the display. The anode controls for the remaining characters, AN[2:0] are all High, and these characters ignore the values presented on A through G and DP.

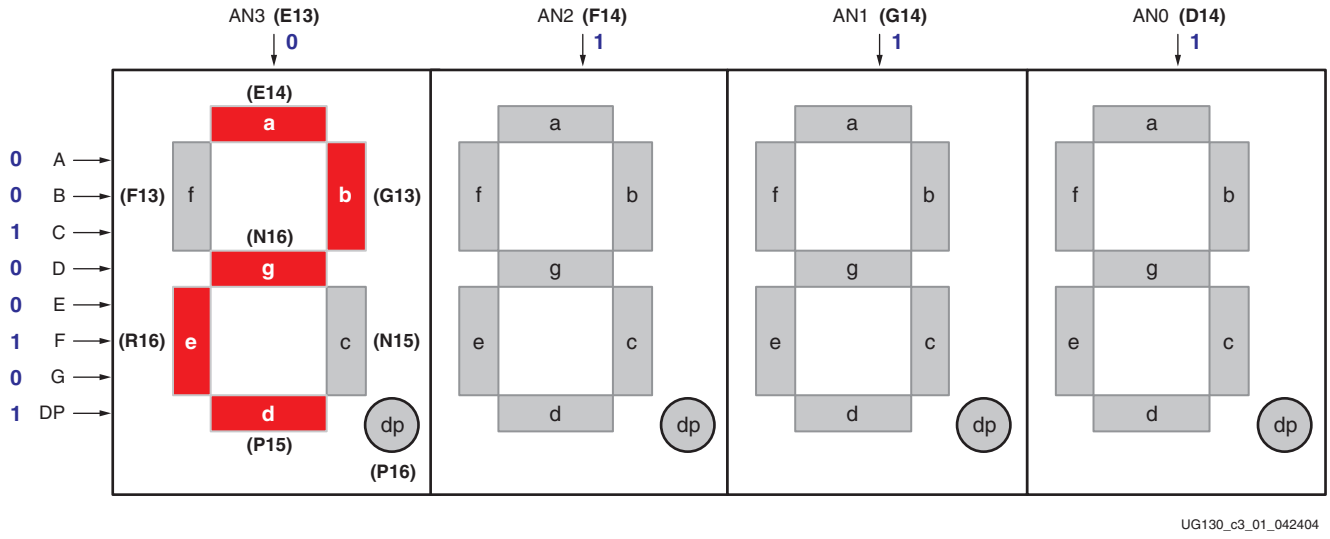



*Figure 3-1:* **Seven-Segment LED Digit Control**

Table 3-1 lists the FPGA connections that drive the individual LEDs comprising a seven-segment character. Table 3-2 lists the connections to enable a specific character. Table 3-3 shows the patterns required to display hexadecimal characters.

*Table 3-1:* **FPGA Connections to Seven-Segment Display (Active Low)**

| Segment | FPGA Pin |
|---|---|
| A | E14 |
| B | G13 |
| C | N15 |
| D | P15 |
| E | R16 |
| F | F13 |
| G | N16 |
| DP | P16 |

*Table 3-2:* **Digit Enable (Anode Control) Signals (Active Low)**

| **Anode Control** | AN3 | AN2 | AN1 | AN0 |
|---|---|---|---|---|
| **FPGA Pin** | E13 | F14 | G14 | D14 |

*Table 3-3:* **Display Characters and Resulting LED Segment Control Values**

| Character | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| A | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| b | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| C | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| d | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| E | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| F | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

The LED control signals are time-multiplexed to display data on all four characters, as shown in Figure 3-2. Present the value to be displayed on the segment control inputs and select the specified character by driving the associated anode control signal Low. Through persistence of vision, the human brain perceives that all four characters appear simultaneously, similar to the way the brain perceives a TV display.

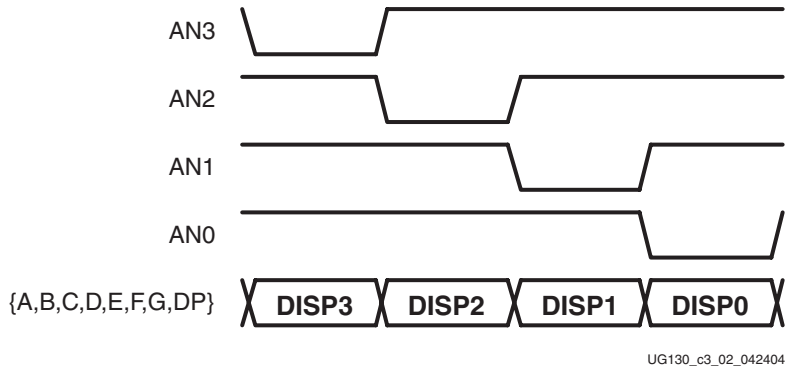



*Figure 3-2:* **Drive Anode Input Low to Light an Individual Character**

This "scanning" technique reduces the number of I/O pins required for the four characters. If an FPGA pin were dedicated for each individual segment, then 32 pins are required to drive four 7-segment LED characters. The scanning technique reduces the required I/O down to 12 pins. The drawback to this approach is that the FPGA logic must continuously scan data out to the displays—a small price to save 20 additional I/O pins.

Chapter 4

# Switches and LEDs

## Slide Switches

The Spartan-3 Starter Kit board has eight slide switches, indicated as (11) in Figure 1-2. The switches are located along the lower edge of the board, toward the right edge. The switches are labeled SW7 through SW0. Switch SW7 is the left-most switch, and SW0 is the right-most switch. The switches connect to an associated FPGA pin, as shown in Table 4-1. A detailed schematic appears in Figure A-2.

*Table 4-1:* **Slider Switch Connections**

| **Switch** | SW7 | SW6 | SW5 | SW4 | SW3 | SW2 | SW1 | SW0 |
|---|---|---|---|---|---|---|---|---|
| **FPGA Pin** | K13 | K14 | J13 | J14 | H13 | H14 | G12 | F12 |

When in the UP or ON position, a switch connects the FPGA pin to $V_{CCO}$, a logic High. When DOWN or in the OFF position, the switch connects the FPGA pin to ground, a logic Low. The switches typically exhibit about 2 ms of mechanical bounce and there is no active debouncing circuitry, although such circuitry could easily be added to the FPGA design programmed on the board. A 4.7KΩ series resistor provides nominal input protection.

## Push Button Switches

The Spartan-3 Starter Kit board has four momentary-contact push button switches, indicated as (13) in Figure 1-2. These push buttons are located along the lower edge of the board, toward the right edge. The switches are labeled BTN3 through BTN0. Push button switch BTN3 is the left-most switch, BTN0 the right-most switch. The push button switches connect to an associated FPGA pin, as shown in Table 4-2. A detailed schematic appears in Figure A-2.

*Table 4-2:* **Push Button Switch Connections**

| **Push Button** | BTN3 (User Reset) | BTN2 | BTN1 | BTN0 |
|---|---|---|---|---|
| **FPGA Pin** | L14 | L13 | M14 | M13 |

Pressing a push button generates a logic High on the associated FPGA pin. Again, there is no active debouncing circuitry on the push button.

The left-most button, BTN3, is also the default User Reset pin. BTN3 electrically behaves identically to the other push buttons. However, when applicable, BTN3 resets the provided reference designs.

# LEDs

The Spartan-3 Starter Kit board has eight individual surface-mount LEDs located above the push button switches, indicated by (12) in Figure 1-2. The LEDs are labeled LED7 through LED0. LED7 is the left-most LED, LED0 the right-most LED. Table 4-3 shows the FPGA connections to the LEDs.

*Table 4-3:* **LED Connections to the Spartan-3 FPGA**

| **LED** | LD7 | LD6 | LD5 | LD4 | LD3 | LD2 | LD1 | LD0 |
|---|---|---|---|---|---|---|---|---|
| **FPGA Pin** | P11 | P12 | N12 | P13 | N14 | L12 | P14 | K12 |

The cathode of each LED connects to ground via a 270Ω resistor. To light an individual LED, drive the associated FPGA control signal High, which is the opposite polarity from lighting one of the 7-segment LEDs.

# VGA Port

The Spartan-3 Starter Kit board includes a VGA display port and DB15 connector, indicated as (5) in Figure 1-2. Connect this port directly to most PC monitors or flat-panel LCD displays using a standard monitor cable.

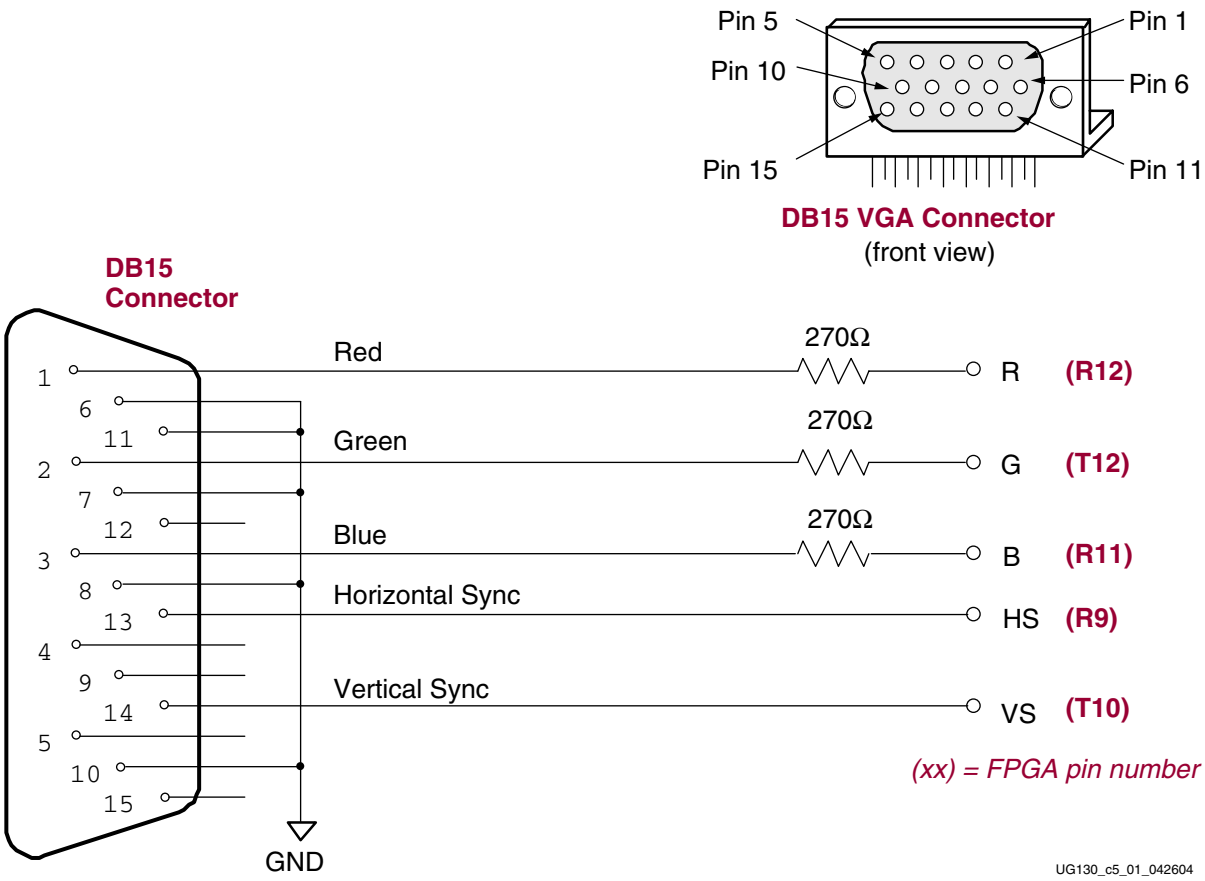



*Figure 5-1:* **VGA Connections from Spartan-3 Starter Kit Board**

As shown in Figure 5-1, the Spartan-3 FPGA controls five VGA signals: Red (R), Green (G), Blue (B), Horizontal Sync (HS), and Vertical Sync (VS), all available on the VGA connector. The FPGA pins that drive the VGA port appear in Table 5-1. A detailed schematic is in Figure A-7.

*Table 5-1:* **VGA Port Connections to the Spartan-3 FPGA**

| Signal | FPGA Pin |
|---|---|
| Red (R) | R12 |
| Green (G) | T12 |
| Blue (B) | R11 |
| Horizontal Sync (HS) | R9 |
| Vertical Sync (VS) | T10 |

Each color line has a series resistor to provide 3-bit color, with one bit each for Red, Green, and Blue. The series resistor uses the 75Ω VGA cable termination to ensure that the color signals remain in the VGA-specified 0V to 0.7V range. The HS and VS signals are TTL level. Drive the R, G, and B signals High or Low to generate the eight possible colors shown in Table 5-2.

*Table 5-2:* **3-Bit Display Color Codes**

| Red (R) | Green (G) | Blue (B) | Resulting Color |
|---|---|---|---|
| 0 | 0 | 0 | **Black** |
| 0 | 0 | 1 | **Blue** |
| 0 | 1 | 0 | **Green** |
| 0 | 1 | 1 | **Cyan** |
| 1 | 0 | 0 | **Red** |
| 1 | 0 | 1 | **Magenta** |
| 1 | 1 | 0 | **Yellow** |
| 1 | 1 | 1 | **White** |

VGA signal timing is specified, published, copyrighted, and sold by the Video Electronics Standards Association (VESA). The following VGA system and timing information is provided as an example of how the FPGA might drive VGA monitor in 640 by 480 mode. For more precise information or for information on higher VGA frequencies, refer to documents available on the VESA website or other electronics websites:

- Video Electronics Standards Association
  http://www.vesa.org
- VGA Timing Information
  http://www.epanorama.net/documents/pc/vga_timing.html

# Signal Timing for a 60Hz, 640x480 VGA Display

CRT-based VGA displays use amplitude-modulated, moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permitivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the

same signal timings as CRT displays. Consequently, the following discussion pertains to both CRTs and LCD displays.

Within a CRT display, current waveforms pass through the coils to produce magnetic fields that deflect electron beams to transverse the display surface in a “raster” pattern, horizontally from left to right and vertically from top to bottom. As shown in Figure 5-2, information is only displayed when the beam is moving in the “forward” direction—left to right and top to bottom—and not during the time the beam returns back to the left or top edge of the display. Much of the potential display time is therefore lost in “blanking” periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass.

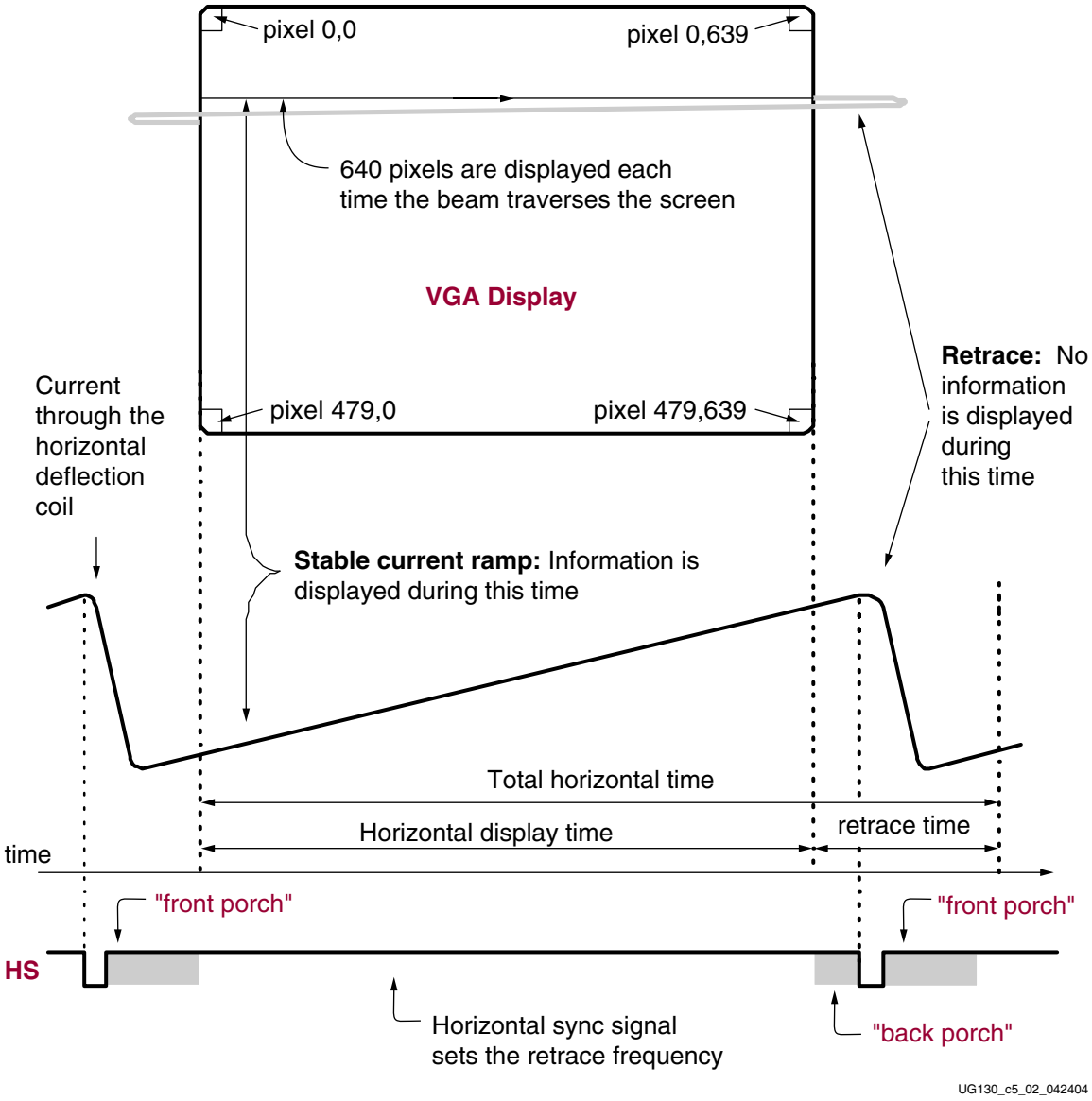



*Figure 5-2:* **CRT Display Timing Example**

The size of the beams, the frequency at which the beam traces across the display, and the frequency at which the electron beam is modulated determine the display resolution.

Modern VGA displays support multiple display resolutions, and the VGA controller dictates the resolution by producing timing signals to control the raster patterns. The controller produces TTL-level synchronizing pulses that set the frequency at which current flows through the deflection coils, and it ensures that pixel or video data is applied to the electron guns at the correct time.

Video data typically comes from a video refresh memory with one or more bytes assigned to each pixel location. The Spartan-3 Starter Kit board uses three bits per pixel, producing one of the eight possible colors shown in Table 5-2. The controller indexes into the video data buffer as the beams move across the display. The controller then retrieves and applies video data to the display at precisely the time the electron beam is moving across a given pixel.

As shown in Figure 5-2, the VGA controller generates the HS (horizontal sync) and VS (vertical sync) timings signals and coordinates the delivery of video data on each pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies in the 60 Hz to 120 Hz range. The number of horizontal lines displayed at a given refresh frequency defines the horizontal "retrace" frequency.

## VGA Signal Timing

The signal timings in Table 5-3 are derived for a 640-pixel by 480-row display using a 25 MHz pixel clock and 60 Hz ±1 refresh. Figure 5-3 shows the relation between each of the timing symbols. The timing for the sync pulse width ($T_{PW}$) and front and back porch intervals ($T_{FP}$ and $T_{BP}$) are based on observations from various VGA displays. The front and back porch intervals are the pre- and post-sync pulse times. Information cannot be displayed during these times.

*Table 5-3:* **640x480 Mode VGA Timing**

| Symbol | Parameter | Vertical Sync | | | Horizontal Sync | |
|---|---|---|---|---|---|---|
| | | Time | Clocks | Lines | Time | Clocks |
| $T_S$ | Sync pulse time | 16.7 ms | 416,800 | 521 | 32 µs | 800 |
| $T_{DISP}$ | Display time | 15.36 ms | 384,000 | 480 | 25.6 µs | 640 |
| $T_{PW}$ | Pulse width | 64 µs | 1,600 | 2 | 3.84 µs | 96 |
| $T_{FP}$ | Front porch | 320 µs | 8,000 | 10 | 640 ns | 16 |
| $T_{BP}$ | Back porch | 928 µs | 23,200 | 29 | 1.92 µs | 48 |

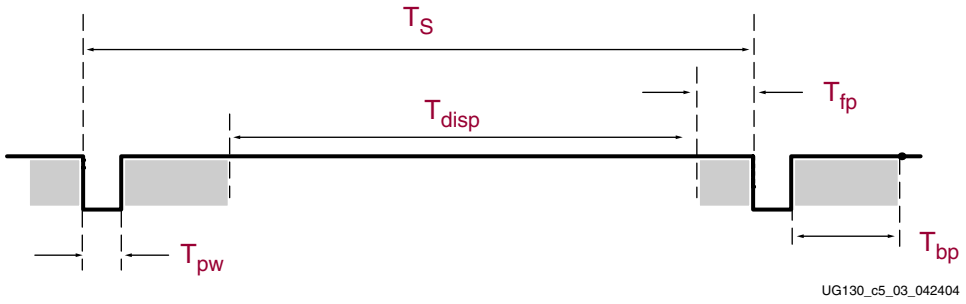



*Figure 5-3:* **VGA Control Timing**

Generally, a counter clocked by the pixel clock controls the horizontal timing. Decoded counter values generate the HS signal. This counter tracks the current pixel display location on a given row.

A separate counter tracks the vertical timing. The vertical-sync counter increments with each HS pulse and decoded values generate the VS signal. This counter tracks the current display row. These two continuously running counters form the address into a video display buffer. For example, the on-board fast SRAM is an ideal display buffer.

No time relationship is specified between the onset of the HS pulse and the onset of the VS pulse. Consequently the counters can be arranged to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

Chapter 6

# PS/2 Mouse/Keyboard Port

The Spartan-3 Starter Kit board includes a PS/2 mouse/keyboard port and the standard 6-pin mini-DIN connector, labeled J3 on the board and indicated as (9) in Figure 1-2. Figure 6-1 shows the PS/2 connector, and Table 6-1 shows the signals on the connector. Only pins 1 and 5 of the connector attach to the FPGA. A detailed schematic appears in Figure A-7.

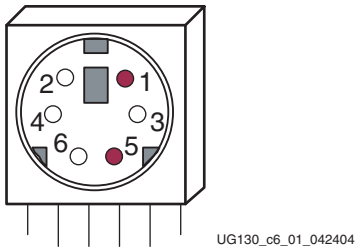



*Figure 6-1:* **PS/2 DIN Connector**

*Table 6-1:* **PS/2 Connections to the Spartan-3 FPGA**

| PS/2 DIN Pin | Signal | FPGA Pin |
|---|---|---|
| 1 | DATA (PS2D) | M15 |
| 2 | Reserved | — |
| 3 | GND | GND |
| 4 | Voltage Supply | — |
| 5 | CLK (PS2C) | M16 |
| 6 | Reserved | — |

Both a PC mouse and keyboard use the two-wire PS/2 serial bus to communicate with a host device, the Spartan-3 FPGA in this case. The PS/2 bus includes both clock and data. Both a mouse and keyboard drive the bus with identical signal timings and both use 11-bit words that include a start, stop and odd parity bit. However, the data packets are organized differently for a mouse and keyboard. Furthermore, the keyboard interface allows bidirectional data transfers so the host device can illuminate state LEDs on the keyboard.

The PS/2 bus timing appears Table 6-2 and Figure 6-2. The clock and data signals are only driven when data transfers occur, and otherwise they are held in the idle state at logic

High. The timings define signal requirements for mouse-to-host communications and bidirectional keyboard communications.

*Table 6-2:* **PS/2 Bus Timing**

| Symbol | Parameter | Min | Max |
|---|---|---|---|
| $T_{CK}$ | Clock High or Low time | 30 µs | 50 µs |
| $T_{SU}$ | Data-to-clock setup time | 5 µs | 25 µs |
| $T_{HLD}$ | Clock-to-data hold time | 5 µs | 25 µs |

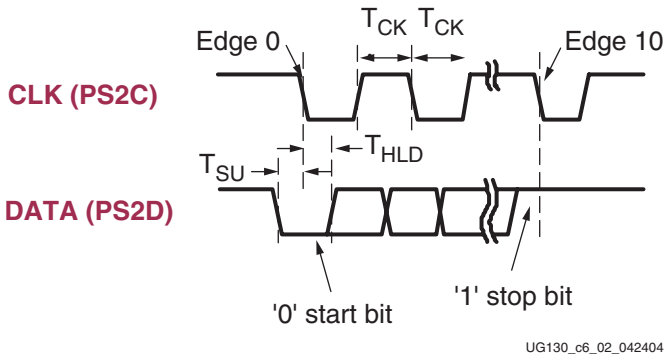



*Figure 6-2:* **PS/2 Bus Timing Waveforms**

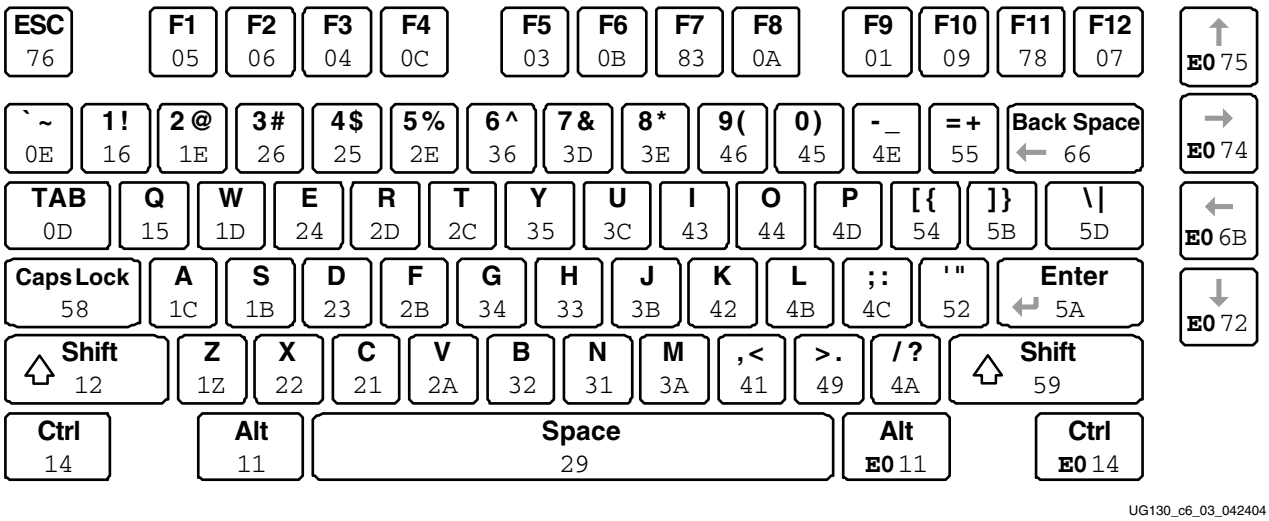
# Keyboard

The keyboard uses open-collector drivers so that either the keyboard or the host can drive the two-wire bus. If the host never sends data to the keyboard, then the host can use simple input pins.

A PS/2-style keyboard uses scan codes to communicate key press data. Nearly all keyboards in use today are PS/2 style. Each key has a single, unique scan code that is sent whenever the corresponding key is pressed. The scan codes for most keys appear in Figure 6-3.

If the key is pressed and held, the keyboard repeatedly sends the scan code every 100 ms or so. When a key is released, the keyboard sends a “F0” key-up code, followed by the scan code of the released key. The keyboard sends the same scan code, regardless if a key has different “shift” and “non-shift” characters and regardless whether the Shift key is pressed or not. The host determines which character is intended.

Some keys, called extended keys, send an “E0” ahead of the scan code and furthermore, they may send more than one scan code. When an extended key is released, a “E0 F0” key-up code is sent, followed by the scan code.




UG130_c6_03_042404

*Figure 6-3:* **PS/2 Keyboard Scan Codes**

The host can also send data to the keyboard. Table 6-3 provides a short list of some often-used commands.

*Table 6-3:* **Common PS/2 Keyboard Commands**

| Command | Description |
|---|---|
| ED | Turn on/off Num Lock, Caps Lock, and Scroll Lock LEDs. The keyboard acknowledges receipt of an "ED" command by replying with an "FA", after which the host sends another byte to set LED status. The bit positions for the keyboard LEDs appear in Table 6-4. Write a '1' to the specific bit to illuminate the associated keyboard LED. |
| EE | Echo. Upon receiving an echo command, the keyboard replies with the same scan code "EE". |
| F3 | Set scan code repeat rate. The keyboard acknowledges receipt of an "F3" by returning an "FA", after which the host sends a second byte to set the repeat rate. |
| FE | Resend. Upon receiving a resend command, the keyboard resends the last scan code sent. |
| FF | Reset. Resets the keyboard. |

*Table 6-4:* **Keyboard LED Control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Ignored | | | | | Caps Lock | Num Lock | Scroll Lock |

The keyboard sends data to the host only when both the data and clock lines are High, the Idle state.

Because the host is the "bus master", the keyboard checks whether the host is sending data before driving the bus. The clock line can be used as a "clear to send" signal. If the host pulls the clock line Low, the keyboard must not send any data until the clock is released.

The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by eight bits of scan code (LSB first), followed by an odd parity bit and terminated with a '1' stop bit. When the keyboard sends data, it generates 11 clock transitions at around 20 to 30 kHz, and data is valid on the falling edge of the clock as shown in Figure 6-2.

# Mouse

A mouse generates a clock and data signal when moved; otherwise, these signals remain High indicating the Idle state. Each time the mouse is moved, the mouse sends three 11-bit words to the host. Each of the 11-bit words contains a '0' start bit, followed by 8 data bits (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Each data transmission contains 33 total bits, where bits 0, 11, and 22 are '0' start bits, and bits 10, 21, and 32 are '1' stop bits. The three 8-bit data fields contain movement data as shown in Figure 6-4. Data is valid at the falling edge of the clock, and the clock period is 20 to 30 kHz.

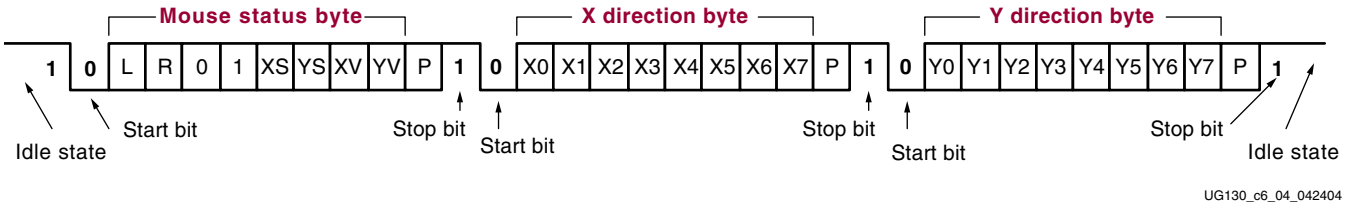



*Figure 6-4:* **PS/2 Mouse Transaction**

As shown in Figure 6-5, a PS/2 mouse employs a relative coordinate system wherein moving the mouse to the right generates a positive value in the X field, and moving to the left generates a negative value. Likewise, moving the mouse up generates a positive value in the Y field, and moving down represents a negative value. The XS and YS bits in the status byte define the sign of each value, where a '1' indicates a negative value.

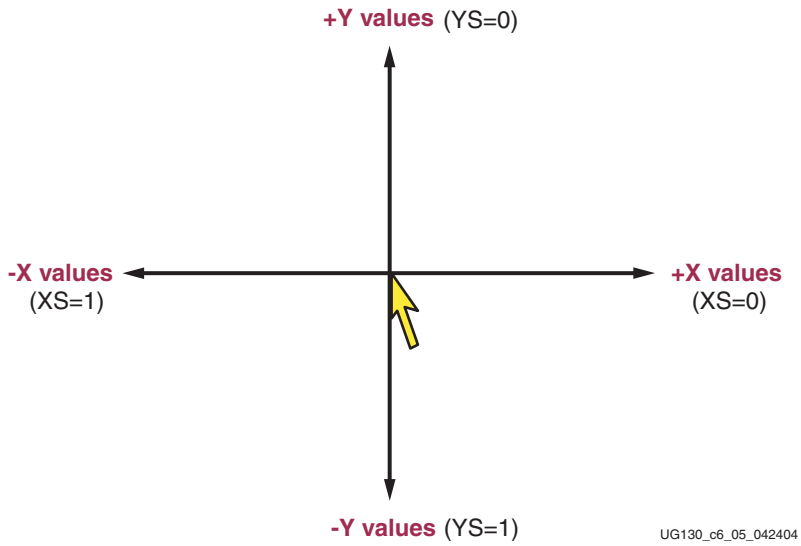



*Figure 6-5:* **The Mouse Uses a Relative Coordinate System to Track Movement**

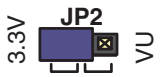
The magnitude of the X and Y values represent the rate of mouse movement. The larger the value, the faster the mouse is moving. The XV and YV bits in the status byte indicate when the X or Y values exceed their maximum value, an overflow condition. A '1' indicates when an overflow occurs. If the mouse moves continuously, the 33-bit transmissions repeat every 50 ms or so.

The L and R fields in the status byte indicate Left and Right button presses. A '1' indicates that the associated mouse button is being pressed.

# Voltage Supply

Most modern keyboards and mice work equally well from a 3.3V or 5V supply. The voltage supply for the PS/2 port is selectable via the JP2 jumper, indicated as (30) in Figure 1-2, located immediately above the PS/2 connector along the right edge. The 3.3V setting is preferred as the FPGA's output signals operate from the 3.3V supply. The JP2 jumper should be positioned as shown in Table 6-5 by default.

*Table 6-5:* **PS/2 Port Supply Voltage Options**

| PS/2 Port Supply Voltage | Jumper JP2 Setting |
|---|---|
| 3.3V |   |
| 5V | |

Some older keyboards and mice are 5V only. Consequently, the JP2 jumper should be set for 5V operation as shown in Table 6-5. The Spartan-3 FPGA can tolerate 5V signals due to the 270Ωseries resistors on the PS/2 data and clock signals connected to the FPGA. See the schematic in Figure A-7 for more details.

# RS-232 Port

The Spartan-3 Starter Kit board has an RS-232 serial port. The RS-232 transmit and receive signals appear on the female DB9 connector, labeled J2, indicated as (6) in Figure 1-2. The connector is a DCE-style port and connects to the DB9 DTE-style serial port connector available on most personal computers and workstations. Use a standard straight-through serial cable to connect the Spartan-3 Starter Kit board to the PC's serial port.

Figure 7-1 shows the connection between the FPGA and the DB9 connector, including the Maxim MAX3232 RS-232 voltage converter, indicated as (7) in Figure 1-2. The FPGA supplies serial output data as LVTLL or LVCMOS levels to the Maxim device, which in turn, converts the logic value to the appropriate RS-232 voltage level. Likewise, the Maxim device converts the RS-232 serial input data to LVTLL levels for the FPGA. A series resistor between the Maxim output pin and the FPGA's RXD pin protects against accidental logic conflicts. A detailed schematic appears in Figure A-7.

Hardware flow control is not supported on the connector. The port's DCD, DTR, and DSR signals connect together, as shown in Figure 7-1. Similarly, the port's RTS and CTS signals connect together.

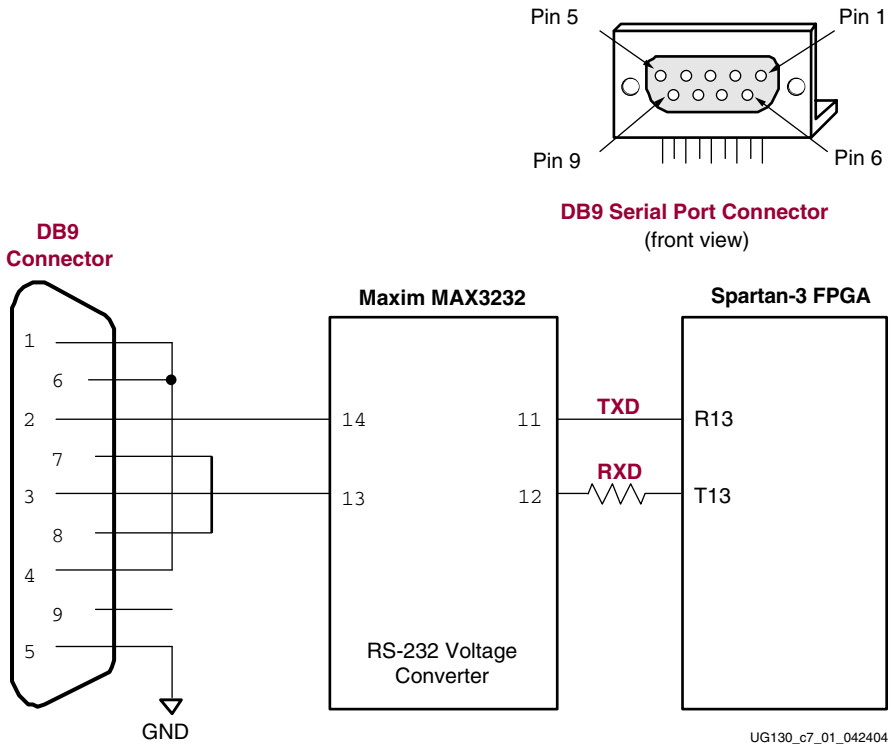



*Figure 7-1:* **RS-232 Serial Port**

The FPGA connections to the Maxim RS-232 translator appear in Table 7-1.

*Table 7-1:* **Accessory Port Connections to the Spartan-3 FPGA**

| Signal | FPGA Pin |
|---|---|
| RXD | T13 |
| TXD | R13 |
| RXD-A | N10 |
| TXD-A | T14 |

An auxiliary RS-232 serial channel from the Maxim device is available on two 0.1-inch stake pins, indicated as J1 in the schematic and (8) in Figure 1-2. The FPGA connections driving the Maxim device appear in Table 7-1 with signals RXD-A and TXD-A.

Chapter 8

# Clock Sources

The Spartan-3 Starter Kit board has a dedicated 50 MHz Epson SG-8002JF series clock oscillator source and an optional socket for another clock oscillator source. Figure A-5 provides a detailed schematic for the clock sources.

The 50 MHz clock oscillator is mounted on the bottom side of the board, indicated as (14) in Figure A-5. Use the 50 MHz clock frequency as is or derive other frequencies using the FPGAs Digital Clock Managers (DCMs).

- Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs
  http://www.xilinx.com/bvdocs/appnotes/xapp462.pdf

The oscillator socket, indicated as (15) in Figure 1-2, accepts oscillators in an 8-pin DIP footprint.

*Table 8-1:* **Clock Oscillator Sources**

| Oscillator Source | FPGA Pin |
|---|---|
| 50 MHz (IC4) | T9 |
| Socket (IC8) | D9 |

Chapter 9

# FPGA Configuration Modes and Functions

## FPGA Configuration Mode Settings

In most applications for the Spartan-3 Starter Kit Board, the FPGA automatically boots from the on-board Platform Flash memory whenever power is applied or the PROG push button is pressed. However, the board supports all the available configuration modes via the J8 header, indicated as (16) in Figure 1-2. Table 9-1 provides the available option settings for the J8 header. Additionally, the JP1 jumper setting is required when using Master Serial configuration mode, as further described in "Platform Flash Jumper Options (JP1)."

The default jumper settings for the board are:

- All jumpers in the J8 header are installed
- The JP1 jumper is in the "Default" position

*Table 9-1:* **Header J8 Controls the FPGA Configuration Mode**

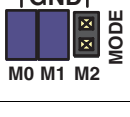
| Configuration Mode <M0:M1:M2> | Header J8 Settings | Jumper JP1 Setting | Description |
|---|---|---|---|
| Master Serial <0:0:0> | | | **DEFAULT**. The FPGA automatically boots from the Platform Flash. |
| | | | The FPGA attempts to boot from a serial configuration source attached to either expansion connector A2 or B1. |
| Slave Serial <1:1:1> | | | Another device connected to either the A2 or B1 expansion connector provides serial data and clock to load the FPGA. |
| Master Parallel <1:1:0> |  | | The FPGA attempts to boot from a parallel configuration source attached to the B1 expansion connector. |

*Table 9-1:* **Header J8 Controls the FPGA Configuration Mode *(Continued)***

| Configuration Mode <M0:M1:M2> | Header J8 Settings | Jumper JP1 Setting | Description |
|---|---|---|---|
| Slave Parallel <0:1:1> | | | Another device connected to the B1 expansion connector provides parallel data and clock to load the FPGA. |
| JTAG <1:0:1> | | | The FPGA waits for configuration via the four-wire JTAG interface. |

# Program Push Button/DONE Indicator LED

The Spartan-3 Starter Kit Board includes two FPGA configuration functions, located near the VGA connector and the AC power input connector, as shown in Figure 9-1. The PROG push button, shown as (17) in Figure 9-1, drives the FPGA's PROG_B programming pin. When pressed, the PROG push button forces the FPGA to reconfigure and reload it configuration data.

The DONE LED, shown as (18) in Figure 9-1, connects to the FPGA's DONE pin and lights up when the FPGA is successfully configured.

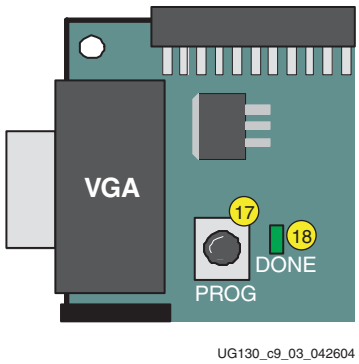



*Figure 9-1:* **The PROG Button and the DONE LED**

Chapter 10

# Platform Flash Configuration Storage

The Spartan-3 Starter Kit board has an XCF02S serial configuration Flash PROM to store FPGA configuration data and potentially additional non-volatile data, including MicroBlaze application code. To configure the FPGA from Platform Flash memory, all three jumpers must be installed on the J8 header, indicated as (16) in Figure 1-2.

## Platform Flash Jumper Options (JP1)

The Platform Flash has three optional settings controlled by the JP1 jumper, which is located in the upper right-hand corner of the board, adjacent to the Platform Flash configuration PROM. The JP1 jumper is indicated as (3) in Figure 1-2. A detailed schematic is provided in Figure A-4. Table 10-1 summarizes the available options, which are described in more detail below.

*Table 10-1:* **Jumper JP1 Controls the Platform Flash Options**

| Option | Jumper JP1 Setting | Description |
|---|---|---|
| **Default** | JP1 | The FPGA boots from Platform Flash. No additional data storage is available. |
| **Flash Read** | JP1 | The FPGA boots from Platform Flash, which is permanently enabled. The FPGA can read additional data from Platform Flash. |
| **Disable** | JP1 | Jumper removed. Platform Flash is disabled. Other configuration data source provides FPGA boot data. |

## "Default" Option

For most applications, this is the default jumper setting. As shown in Figure 10-1, the Platform Flash is enabled only during configuration when the FPGA's DONE pin is Low. When the DONE pin goes High at the end of configuration, the Platform Flash is disabled and placed in low-power mode.

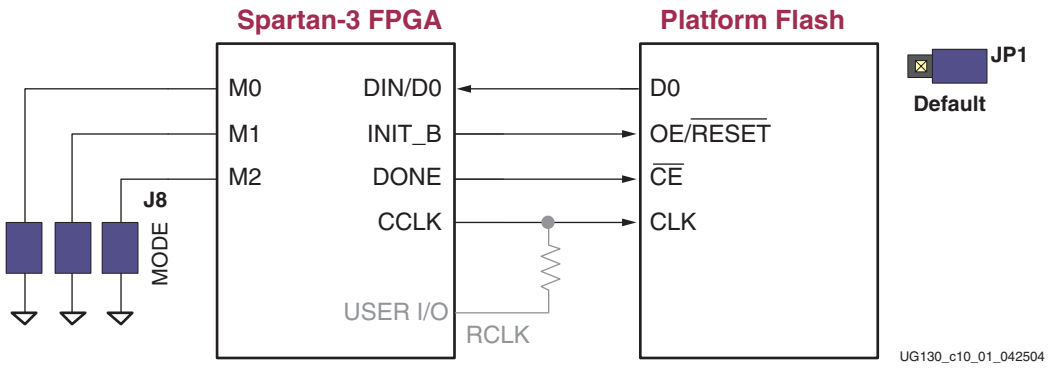



*Figure 10-1:* **Default Platform Flash Option**

# "Flash Read" Option

The Spartan-3 Starter Kit Board includes a 2Mbit Platform Flash configuration PROM. The XC3S200 FPGA on the board only requires slightly less than 1Mbit for configuration data. The remainder of the Platform Flash is available to store other non-volatile data, such as revision codes, serial numbers, coefficients, an Ethernet MAC ID, or code for an embedded processor, such as MicroBlaze, within the FPGA.

To allow the FPGA to read from Platform Flash after configuration, the JP1 jumper must be properly positioned, as shown in Figure 10-2. When the jumper is in this position, the Platform Flash is always enabled. After FPGA configuration completes, the FPGA application drives the INIT_B pin High, FPGA pin N9. Consequently, the Platform Flash data pointer is not reset and points to the additional data following the FPGA configuration data. To read any subsequent data, the FPGA application generates additional clock pulses on the RCLK signal from FPGA pin A14. After configuration, the FPGA's CCLK output is three-stated with a pull-up resistor to $V_{CCAUX}$ (2.5V). The Platform Flash presents serial data on the FPGA's DIN pin, pin M11.

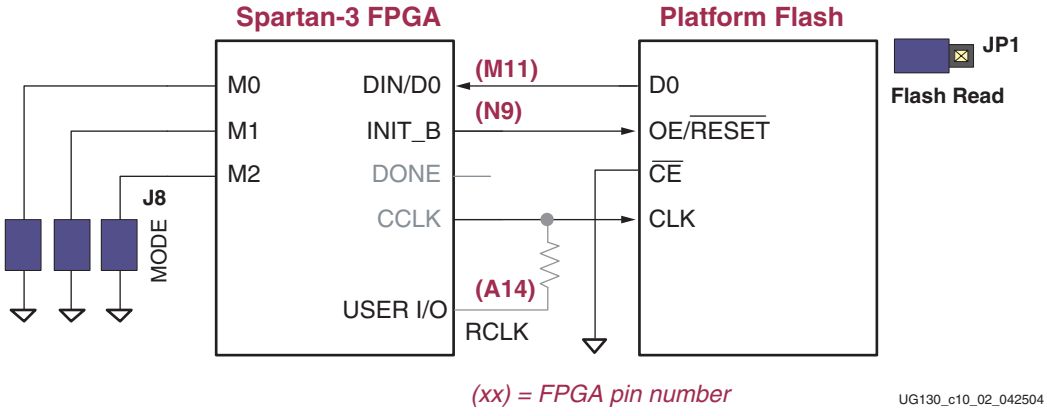



*Figure 10-2:* **Read Additional Data from Platform Flash by Setting the JP1 Jumper**

The resistor between the CCLK output and FPGA pin A14 prevents any accidental conflicts between the two signals.

Additional FPGA logic is required to read the Platform Flash data, as described in the following application note.

- XAPP694: Reading User Data from Configuration PROMs
  http://www.xilinx.com/bvdocs/appnotes/xapp694.pdf

# "Disable" Option

If the JP1 jumper is removed, then the Platform Flash is disabled, potentially allowing configuration via an expansion board connected to one of the expansion connectors.

Chapter 11

# JTAG Programming/Debugging Ports

The Spartan-3 Starter Kit board includes a JTAG programming and debugging chain. Both the Spartan-3 FPGA and the Platform Flash devices are part of the JTAG chain, as shown in Figure 11-1. Additionally, there are two JTAG headers for driving the JTAG signals from various supported JTAG download and debugging cables. A Digilent JTAG3 low-cost parallel to JTAG cable is included as part of the kit and connects to the J7 header.

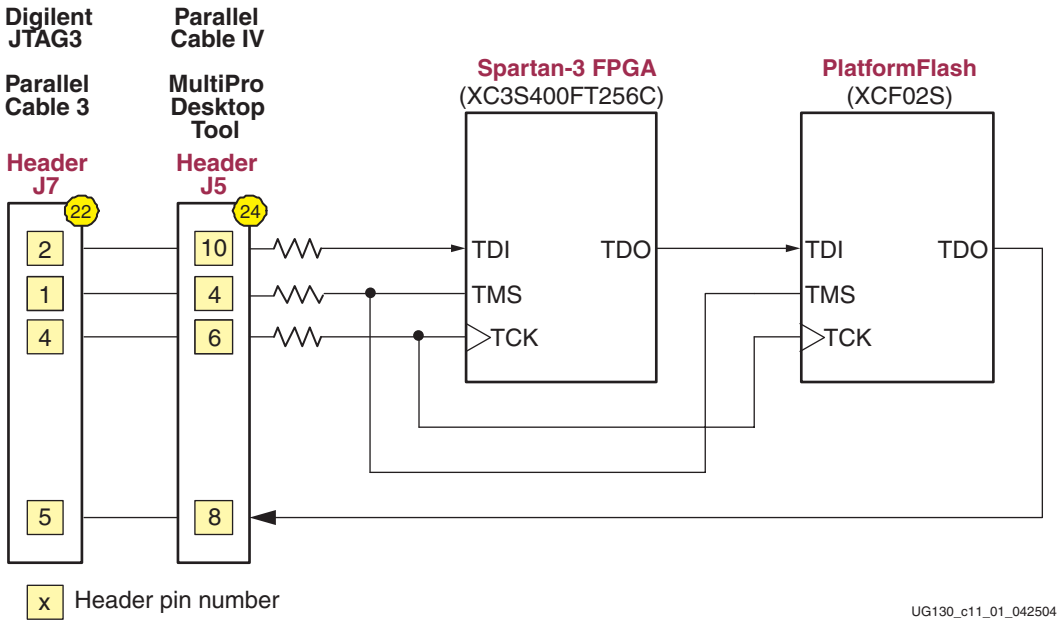



*Figure 11-1:* **Spartan-3 Starter Kit Board JTAG Chain**

## JTAG Header (J7)

This J7 JTAG header consists of 0.1-inch stake pins and is indicated as (22) in Figure 1-2, located toward the top edge of the board, directly below the two expansion connectors. The Digilent low-cost parallel port to JTAG cable fits directly over the J7 header stake pins, as shown in Figure 11-2. When properly fitted, the cable is perpendicular to the board. Make sure that the signals at the end of the JTAG cable align with the labels listed on the board. The other end of the Digilent cable connects to the PC's parallel port. The Digilent cable is directly compatible with the Xilinx iMPACT software. The schematic for the Digilent cable appears in Figure A-9.

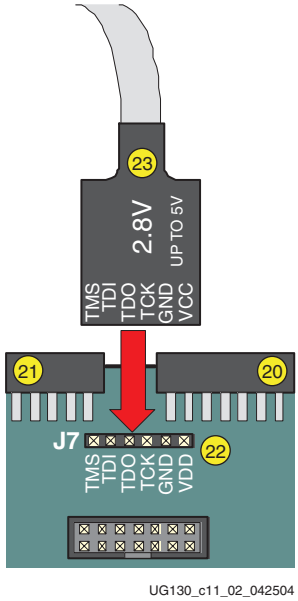



*Figure 11-2:* **Digilent JTAG Cable Provided with Kit Connects to the J7 Header**

The J7 header also supports the Xilinx Parallel Cable 3 (PC3) download / debugging cable when using the flying leaders. Again, make sure that the signals at the end of the JTAG cable align with the labels listed on the board.

Figure A-4 provides a detailed schematic of the J7 header and the JTAG programming chain.

# Parallel Cable IV/MultiPro Desktop Tool JTAG Header (J5)

The J5 header, shown as (24) in Figure 1-2, supports the Xilinx download / debugging cables listed below:

- MultiPro Desktop Tool
  http://www.xilinx.com/bvdocs/publications/ds114.pdf
- Parallel Cable IV (PC IV)
  http://toolbox.xilinx.com/docsan/xilinx4/data/docs/pac/cables6.html

Use the 14-pin ribbon cable supplied with both cables to connect to the J5 header. DO NOT use the flying leads that are also provided with some cables. Although the MultiPro Desktop Tool and the Parallel Cable IV support multiple FPGA configuration modes, the Spartan-3 Starter Kit board only supports the JTAG configuration method. The header is designed for a keyed socket. However, the Spartan-3 Starter Kit uses only stake pins. The outline of the keyed connector appears around the J5 header, as shown in Figure 11-3. When properly inserted, the keyed header matches the outline on the board and the ribbon cable crosses over the top edge of the board. The red-colored lead indicates pin 1 on the cable and should be on the left side.

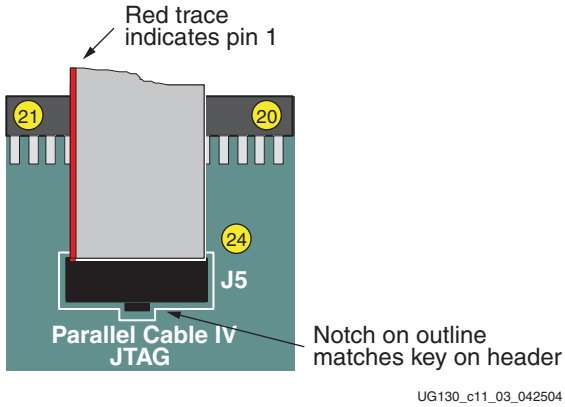



*Figure 11-3:* **Use 14-Pin Ribbon Cable to Connect Parallel Cable IV or the MultiPro Desktop Tool to the J5 Header**

Chapter 12

# Power Distribution

## AC Wall Adapter

The Spartan-3 Starter Kit includes an international-ready AC wall adapter that produces a +5V DC output. Connect the AC wall adapter to the barrel connector along the left edge of the board, indicated as (25) in Figure 1-2. There is no power switch to the board. To disconnect power, remove the AC adapter from the wall or disconnect the barrel connector.

The POWER indicator LED, shown as (26) in Figure 1-2, lights up when power is properly applied to the board. If the jumpers in the J8 header and JP1 header are properly configured and there is a valid design in the Platform Flash memory, then the DONE indicator LED, shown as (18) in Figure 1-2, also lights up.

The AC wall adapter is directly compatible for North America, Japan, and Taiwan locales. Other locations might require a socket adapter to convert from the North American standard to the local power socket standard. The AC wall adapter operates from 100V to 240V AC input, at 50 or 60 Hz.

## Voltage Regulators

There are multiple voltages supplied on the Spartan-3 Starter Kit Board, as summarized in Table 12-1.

*Table 12-1:* **Voltage Supplies and Sources**

| Voltage | Source | Supplies |
|---|---|---|
| +5V DC | AC Wall Adapter, 5V switching power supply ((25) in Figure 1-2) | 3.3V regulator<br>Optionally, PS/2 port via jumper JP2 setting<br>Pin 1 (VU) on A1, A2, B1 expansion connectors |
| +3.3V DC | National Semiconductor LM1086CS-ADJ 3.3V regulator ((27) in Figure 1-2) | 2.5V and 1.2V regulators<br>$V_{CCO}$ supply input for all FPGA I/O banks<br>Most components on the board<br>Pin 3 on A1, A2, B1 expansion connectors |
| +2.5V DC | STMicroelectronics LF25CDT 2.5V regulator ((28) in Figure 1-2) | $V_{CCAUX}$ supply input to FPGA |
| +1.2V DC | 1.2V regulator ((29) in Figure 1-2) | $V_{CCINT}$ supply input to FPGA |

Overall, the 5V DC switching power supply that connects to AC wall power powers the board. A 3.3V regulator, powered by the 5V DC supply, generates power for the 2.5V and

1.2V regulators. Similarly, the 3.3V supply feeds all the $V_{CCO}$ voltage supply inputs to the FPGA's I/O banks and powers most of the components on the board.

The 2.5V regulator, powered by the 3.3V regulator, supplies power to the FPGA's $V_{CCAUX}$ supply inputs. The $V_{CCAUX}$ voltage input supplies power to Digital Clock Managers (DCMs) within the FPGA and supplies some of the I/O structures. In specific, all of the FPGA's dedicated configuration pins, such as DONE, PROG_B, CCLK, and the FPGA's JTAG pins, are powered by $V_{CCAUX}$. The FPGA configuration interface on the board is powered by 3.3V. Consequently, the 2.5V supply has a current shunt resistor to prevent back current.

Finally, a 1.2V regulator supplies power to the FPGA's $V_{CCINT}$ voltage inputs, which power the FPGA's core logic.

The board uses three discrete regulators to generate the necessary voltages. However, various power supply vendors are developing integrated solutions specifically for Spartan-3 FPGAs.

Figure A-3 provides a detailed schematic of the various voltage regulators. Similarly, Figure A-6 shows the power decoupling capacitors.

Chapter 13

# Expansion Connectors and Boards

## Expansion Connectors

The Spartan-3 Starter Kit board has three 40-pin expansion connectors labeled A1, A2, and B1. The A1 and A2 connectors, indicated as (21) and (20), respectively, in Figure 1-2, are on the top edge of the board. Connector A1 is on the top left, and A2 is on the top right. The B1 connector, indicated as (19) in Figure 1-2, is along the left edge of the board.

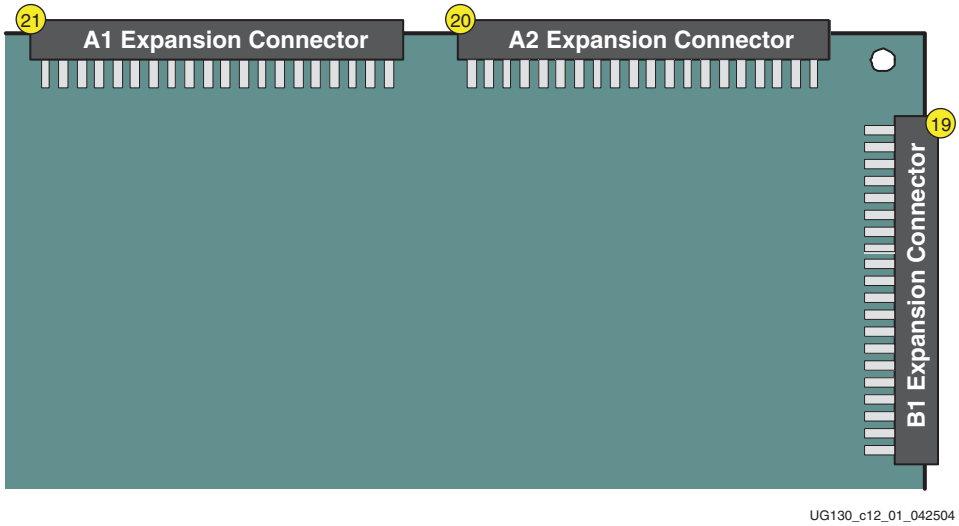



*Figure 13-1:* **Spartan-3 Starter Kit Board Expansion Connectors**

Table 13-1 summarizes the capabilities of each expansion port. Port A1 supports a maximum of 32 user I/O pins, while the other ports provide up to 34 user I/O pins. Some pins are shared with other functions on the board, which may reduce the effective I/O count for specific applications. For example, pins on the A1 port are shared with the SRAM address signals and the SRAM OE# and WE# control signals.

*Table 13-1:* **Expansion Connector Features**

| Connector | User I/O | SRAM Address | JTAG | Serial Configuration | Parallel Configuration |
|---|---|---|---|---|---|
| A1 | 32 | , | , | | |
| A2 | 34 | | | , | |
| B1 | 34 | | | , | , |

Each port offers some ability to program the FPGA on the Spartan-3 Starter Kit Board. For example, port A1 provides additional logic to drive the FPGA and Platform Flash JTAG chain. Similarly, ports A2 and B1 provide connections for Master or Slave Serial mode configuration. Finally, port B1 also offers Master or Slave Parallel configuration mode.

Each 40-pin expansion header, shown in Figure 13-2, uses 0.1-inch (100 mil) DIP spacing. Pin 1 on each connector is always GND. Similarly, pin 2 is always the +5V DC output from the switching power supply. Pin 3 is always the output from the +3.3V DC regulator.

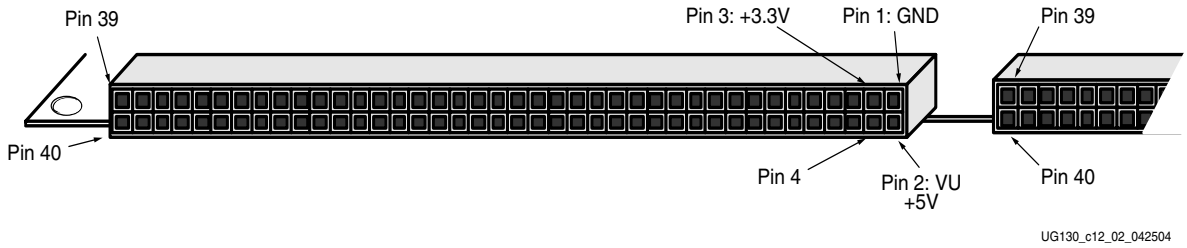



*Figure 13-2:* **40-pin Expansion Connector**

The pinout information for each connector appears below. The tables include the connections between the FPGA and the expansion connectors plus the signal names used in the detailed schematic in Figure A-1.

## A1 Connector Pinout

The A1 expansion connector is located along the top edge of the board, on the left, as indicated by (21) in Figure 1-2. Table 13-2 provides the pinout for the A1 connector. The FPGA connections are specified in parentheses.

*Table 13-2:* **Pinout for A1 Expansion Connector**

| Schematic Name | FPGA Pin | Connector | | FPGA Pin | Schematic Name |
|---|---|---|---|---|---|
| GND | | 1 | 2 | | VU (+5V) |
| $V_{CCO}$ (+3.3V) | $V_{CCO}$ (all banks) | 3 | 4 | (N8) | ADR0 |
| DB0 | (N7) | 5 | 6 | (L5) SRAM A0 | ADR1 |
| DB1 | (T8) | 7 | 8 | (N3) SRAM A1 | ADR2 |
| DB2 | (R6) | 9 | 10 | (M4) SRAM A2 | ADR3 |
| DB3 | (T5) | 11 | 12 | (M3) SRAM A3 | ADR4 |
| DB4 | (R5) | 13 | 14 | (L4) SRAM A4 | ADR5 |
| DB5 | (C2) | 15 | 16 | (G3) SRAM WE# | WE |
| DB6 | (C1) | 17 | 18 | (K4) SRAM OE# | OE |

*Table 13-2:* **Pinout for A1 Expansion Connector *(Continued)***

| Schematic Name | FPGA Pin | Connector | | FPGA Pin | Schematic Name |
|---|---|---|---|---|---|
| DB7 | (B1) | 19 | 20 | (P9)<br>FPGA DOUT/BUSY | CSA |
| LSBCLK | (M7) | 21 | 22 | (M10) | MA1-DB0 |
| MA1-DB1 | (F3)<br>SRAM A6 | 23 | 24 | (G4)<br>SRAM A5 | MA1-DB2 |
| MA1-DB3 | (E3)<br>SRAM A8 | 25 | 26 | (F4)<br>SRAM A7 | MA1-DB4 |
| MA1-DB5 | (G5)<br>SRAM A10 | 27 | 28 | (E4)<br>SRAM A9 | MA1-DB6 |
| MA1-DB7 | (H4)<br>SRAM A12 | 29 | 30 | (H3)<br>SRAM A11 | MA1-ASTB |
| MA1-DSTB | (J3)<br>SRAM A14 | 31 | 32 | (J4)<br>SRAM A13 | MA1-WRITE |
| MA1-WAIT | (K5)<br>SRAM A16 | 33 | 34 | (K3)<br>SRAM A15 | MA1-RESET |
| MA1-INT | (L3)<br>SRAM A17 | 35 | 36 | JTAG Isolation | JTAG Isolation |
| TMS | (C13)<br>FPGA JTAG TMS | 37 | 38 | (C14)<br>FPGA JTAG TCK | TCK |
| TDO-ROM | Platform Flash<br>JTAG TDO | 39 | 40 | Header J7, pin 3 | TDO-A |

The A1 expansion connector shares connections with the 256Kx16 SRAM devices, specifically the SRAM address lines, and the OE# and WE# control signals. Similarly, the JTAG chain is available on pins 36 through 40. Pin 20 is the FPGA DOUT/BUSY configuration signal and toggles during the FPGA configuration process.

## A2 Connector Pinout

The A2 expansion connector is located along the top edge of the board, on the right, as indicated by (20) in Figure 1-2. Figure 13-3 provides the pinout for the A2 connector. The FPGA connections are specified in parentheses.

Most of the A2 expansion connector pins connect only with the FPGA and are not shared. Pin 35 connects to the auxiliary clock socket, if an oscillator is installed in the socket. Pins 36 through 40 include the signals required to configure the FPGA in Master or Slave Serial mode.

*Table 13-3:* **Pinout for A2 Expansion Connector**

| Schematic Name | FPGA Pin | Connector | | FPGA Pin | Schematic Name |
|---|---|---|---|---|---|
| GND | | 1 | 2 | | VU (+5V) |
| $V_{CCO}$ (+3.3V) | $V_{CCO}$ (all banks) | 3 | 4 | (E6) | PA-IO1 |
| PA-IO2 | (D5) | 5 | 6 | (C5) | PA-IO3 |
| PA-IO4 | (D6) | 7 | 8 | (C6) | PA-IO5 |
| PA-IO6 | (E7) | 9 | 10 | (C7) | PA-IO7 |
| PA-IO8 | (D7) | 11 | 12 | (C8) | PA-IO9 |
| PA-IO10 | (D8) | 13 | 14 | (C9) | PA-IO11 |
| PA-IO12 | (D10) | 15 | 16 | (A3) | PA-IO13 |
| PA-IO14 | (B4) | 17 | 18 | (A4) | PA-IO15 |
| PA-IO16 | (B5) | 19 | 20 | (A5) | PA-IO17 |
| PA-IO18 | (B6) | 21 | 22 | (B7) | MA2-DB0 |
| MA2-DB1 | (A7) | 23 | 24 | (B8) | MA2-DB2 |
| MA2-DB3 | (A8) | 25 | 26 | (A9) | MA2-DB4 |
| MA2-DB5 | (B10) | 27 | 28 | (A10) | MA2-DB6 |
| MA2-DB7 | (B11) | 29 | 30 | (B12) | MA2-ASTB |
| MA2-DSTB | (A12) | 31 | 32 | (B13) | MA2-WRITE |
| MA2-WAIT | (A13) | 33 | 34 | (B14) | MA2-RESET |
| MA2-INT/GCK4 | (D9)<br>Oscillator socket | 35 | 36 | (B3)<br>FPGA PROG_B | PROG-B |
| DONE | (R14)<br>FPGA DONE | 37 | 38 | (N9)<br>FPGA INIT_B | INIT |
| CCLK | (T15)<br>FPGA CCLK<br>Connects to (A14) via 390Ω resistor | 39 | 40 | (M11) | DIN |

## B1 Connector Pinout

The B1 expansion connector is located on the right edge of the board, as indicated by (19) in Figure 1-2. Table 13-4 provides the pinout for the B1 connector. The FPGA connections are specified in parentheses.

Most of the B1 expansion connector pins connect only with the FPGA and are not shared. Pins 36 through 40 include the signals required to configure the FPGA in Master or Slave Serial mode. These same pins plus pins 5, 7, 9, 11, 13, 15, 17, 19, and 20 provide the signals required to configure the FPGA in Master or Slave Parallel mode.

*Table 13-4:* **Pinout for B1 Expansion Connector**

| Schematic Name | FPGA Pin | Connector | | FPGA Pin | Schematic Name |
|---|---|---|---|---|---|
| GND | | 1 | 2 | | VU (+5V) |
| $V_{CCO}$ (+3.3V) | $V_{CCO}$ (all banks) | 3 | 4 | (C10) | PB-ADR0 |
| PB-DB0 | (T3)<br>FPGA RD_WR_B config | 5 | 6 | (E10) | PB-ADR1 |
| PB-DB1 | (N11)<br>FPGA D1 config | 7 | 8 | (C11) | PB-ADR2 |
| PB-DB2 | (P10)<br>FPGA D2 config | 9 | 10 | (D11) | PB-ADR3 |
| PB-DB3 | (R10)<br>FPGA D3 config | 11 | 12 | (C12) | PB-ADR4 |
| PB-DB4 | (T7)<br>FPGA D4 config | 13 | 14 | (D12) | PB-ADR5 |
| PB-DB5 | (R7)<br>FPGA D5 config | 15 | 16 | (E11) | PB-WE |
| PB-DB6 | (N6)<br>FPGA D6 config | 17 | 18 | (B16) | PB-OE |
| PB-DB7 | (M6)<br>FPGA D7 config | 19 | 20 | (R3)<br>FPGA CS_B config | PB-CS |
| PB-CLK | (C15) | 21 | 22 | (C16) | MB1-DB0 |
| MB1-DB1 | (D15) | 23 | 24 | (D16) | MB1-DB2 |
| MB1-DB3 | (E15) | 25 | 26 | (E16) | MB1-DB4 |
| MB1-DB5 | (F15) | 27 | 28 | (G15) | MB1-DB6 |
| MB1-DB7 | (G16) | 29 | 30 | (H15) | MB1-ASTB |
| MB1-DSTB | (H16) | 31 | 32 | (J16) | MB1-WRITE |
| MB1-WAIT | (K16) | 33 | 34 | (K15) | MB1-RESET |
| MB1-INT | (L15) | 35 | 36 | (B3)<br>FPGA PROG_B | PROG-B |
| DONE | (R14)<br>FPGA DONE | 37 | 38 | (N9)<br>FPGA INIT_B | INIT |
| CCLK | (T15)<br>FPGA CCLK<br>Connects to (A14) via<br>390Ω resistor | 39 | 40 | (M11) | DIN |

# Expansion Boards

Various expansion boards plug into the A1, A2, or B1 connectors as listed below:

- Spartan-3 Starter Kit Expansion Boards
  http://www.xilinx.com/s3boards
- Digilent Expansion Boards
  https://digilent.us/Sales/boards.cfm#Peripheral
- Digilent Breakout Probe Header (TPH1)
  https://digilent.us/Sales/Product.cfm?Prod=TPH1
- Digilent Breadboard (DBB1)
  https://digilent.us/Sales/Product.cfm?Prod=DBB1
- Digilent Wire-wrap Board (DWR1)
  https://digilent.us/Sales/Product.cfm?Prod=DWR1
- Digilent SPP, EPP, ECP Parallel Port (PIO1)
  https://digilent.us/Sales/Product.cfm?Prod=PIO1

Appendix A

# Board Schematics

This appendix provides the schematics for the Spartan-3 Starter Kit Board:

- Figure A-1, "A1, A2, and B1 Expansion Connectors"
- Figure A-2, "Slide Switches, Push Buttons, LEDs, and Four-Character 7-Segment Display"
- Figure A-3, "Voltage Regulators, JP2 Jumper Setting for PS/2 Port Voltage"
- Figure A-4, "FPGA Configuration Interface, Platform Flash, JTAG Connections, Jumper JP1"
- Figure A-5, "FPGA I/O Connections, Clock Sources"
- Figure A-6, "Power Decoupling Capacitors"
- Figure A-7, "RS-232 Serial Port, VGA Port, PS/2 Port, Parallel Cable IV JTAG Interface"
- Figure A-8, "2x256Kx16 Fast Asynchronous SRAM Interface"
- Figure A-9, "Digilent JTAG3 Low-Cost JTAG Download/Debug Cable"

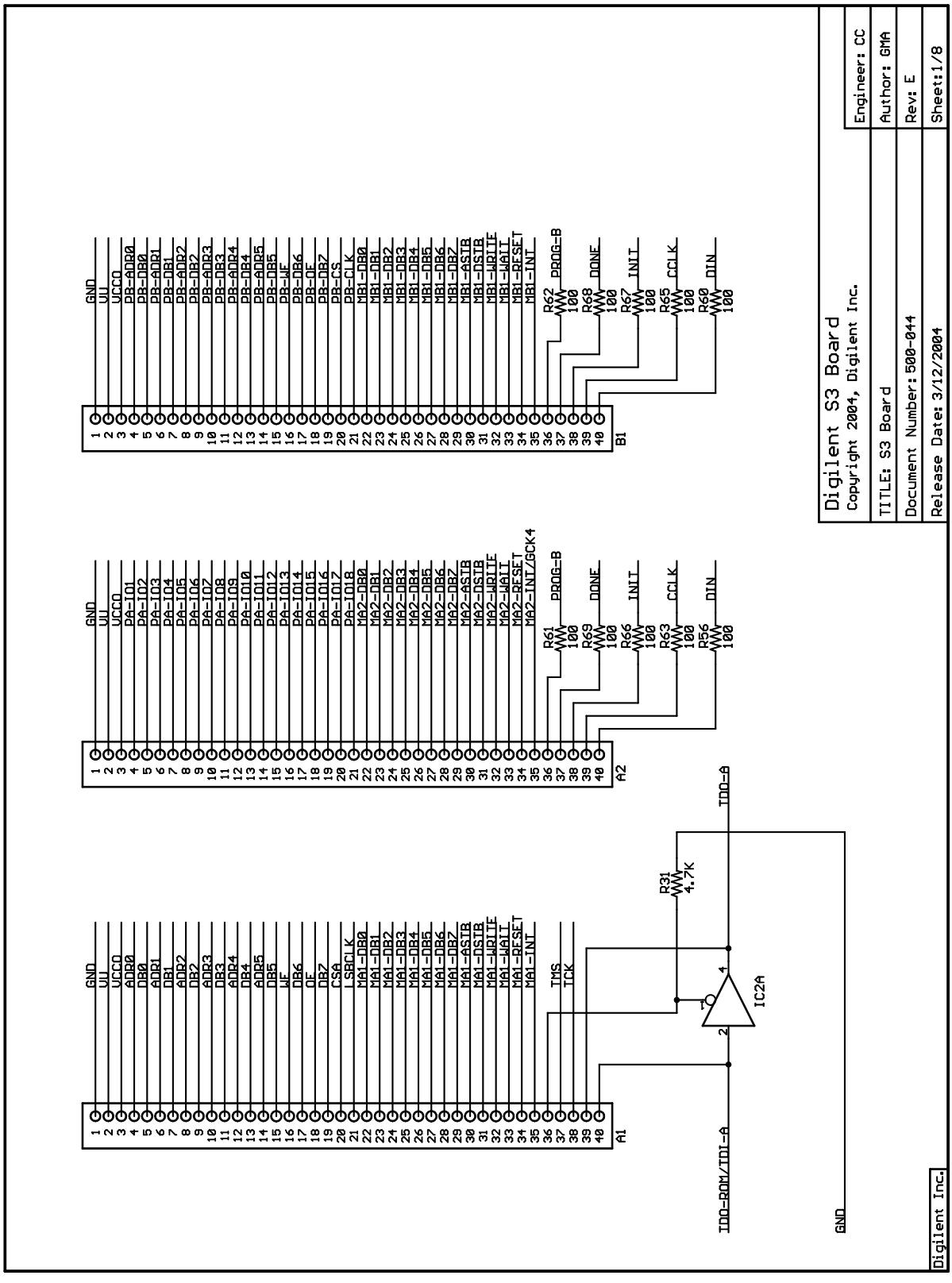



*Figure A-1:* **A1, A2, and B1 Expansion Connectors**

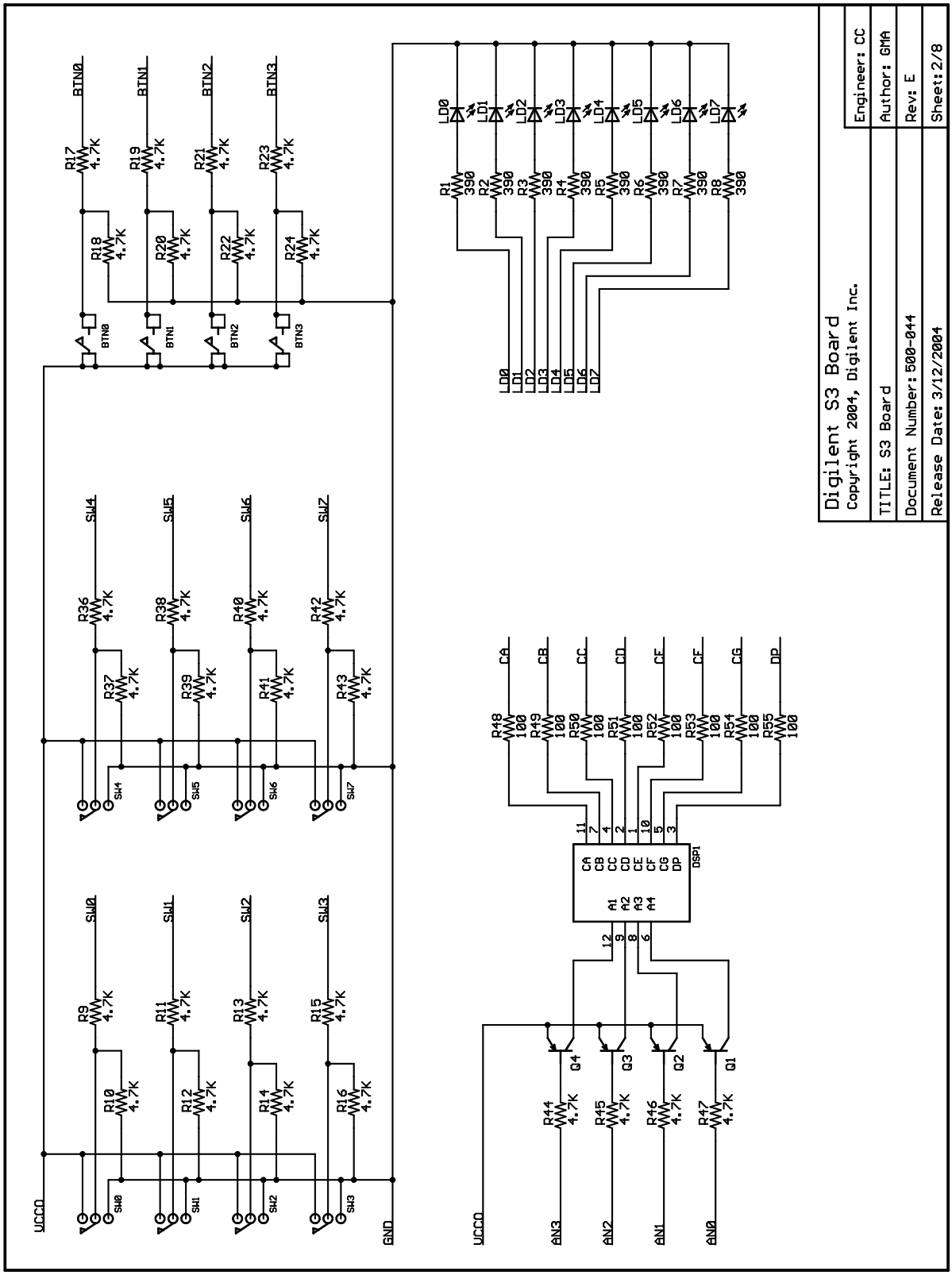



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*Figure A-2:* **Slide Switches, Push Buttons, LEDs, and Four-Character 7-Segment Display**

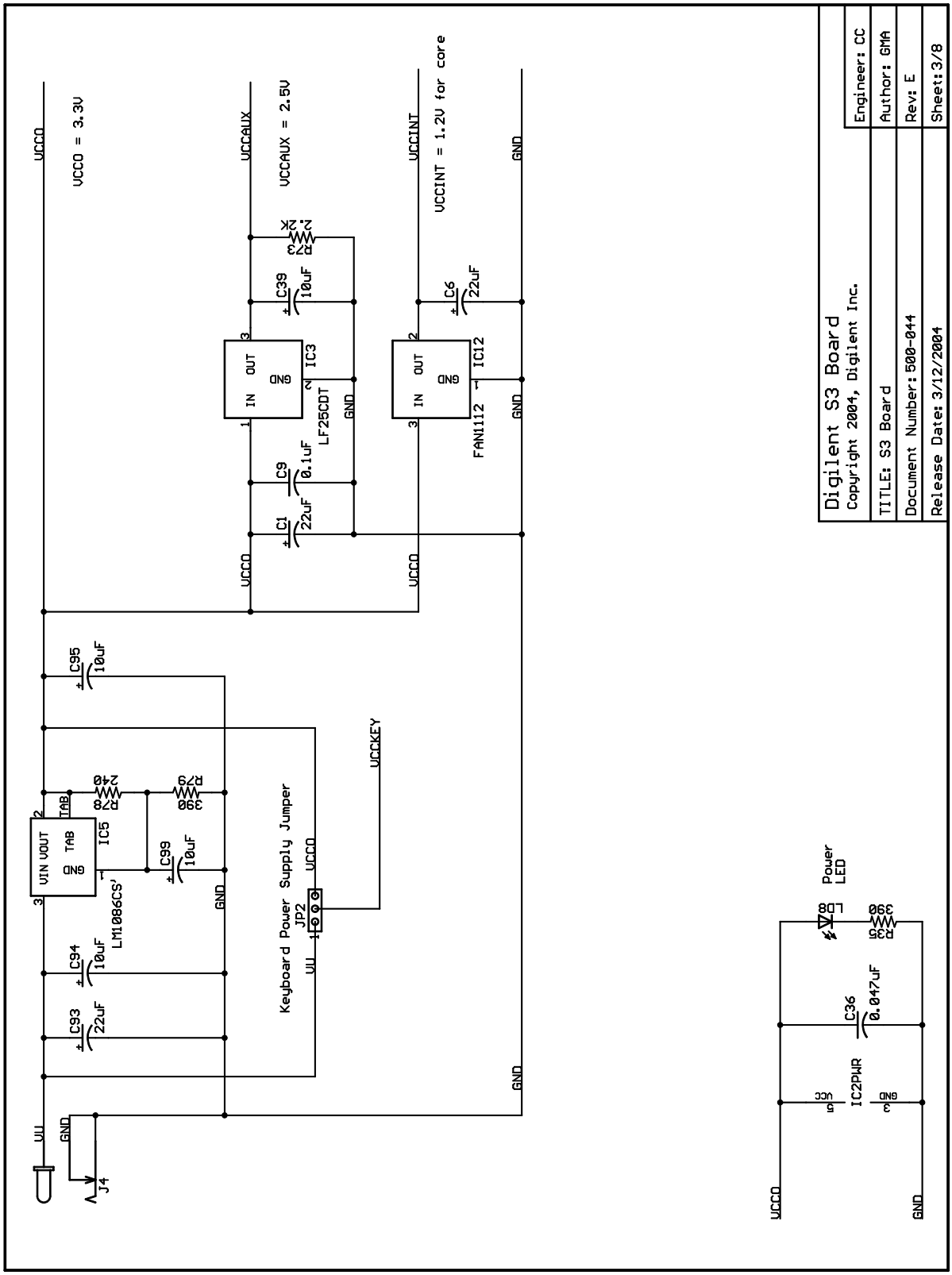


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*Figure A-3:* **Voltage Regulators, JP2 Jumper Setting for PS/2 Port Voltage**

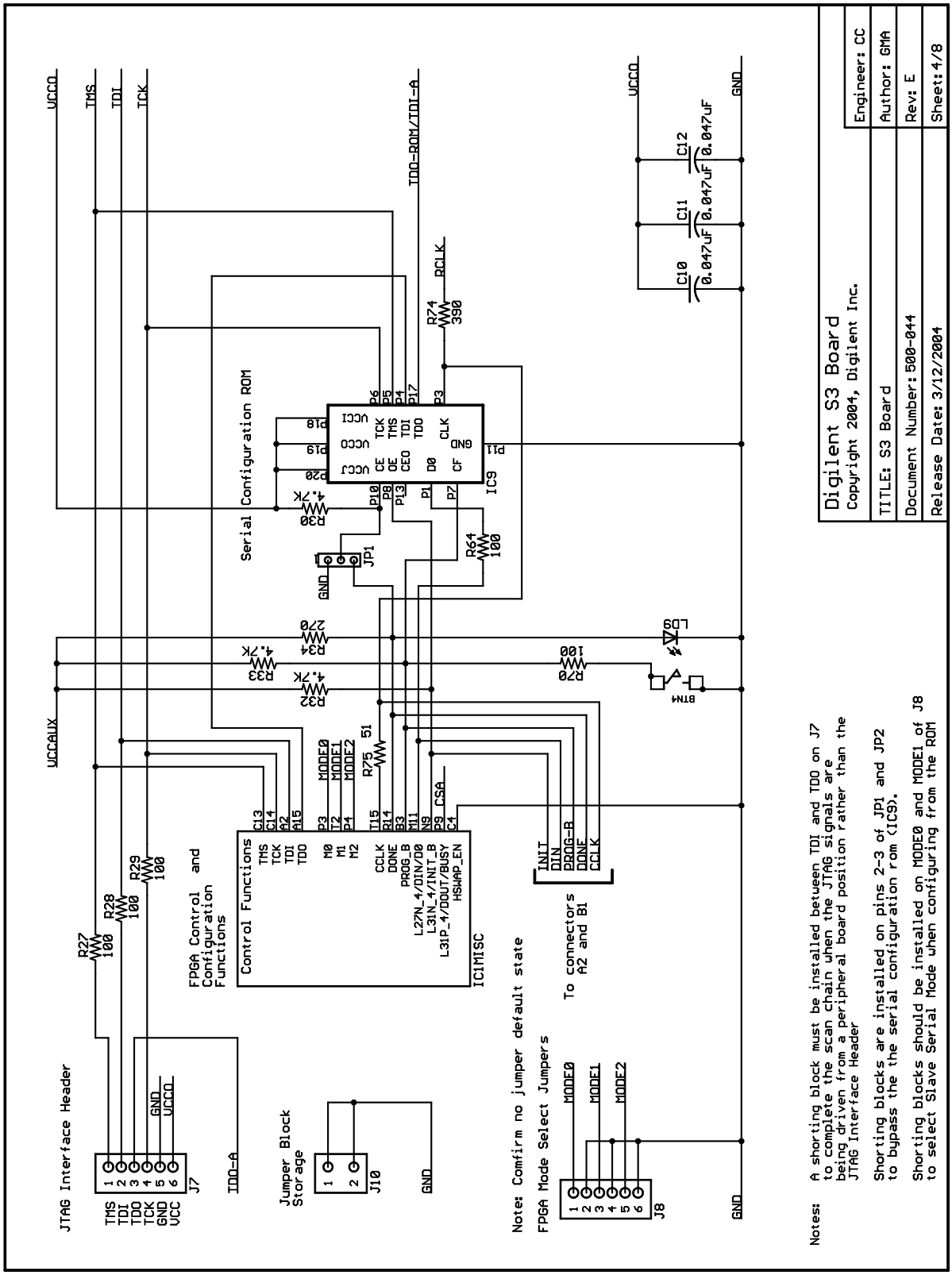


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*Figure A-4:* **FPGA Configuration Interface, Platform Flash, JTAG Connections, Jumper JP1**

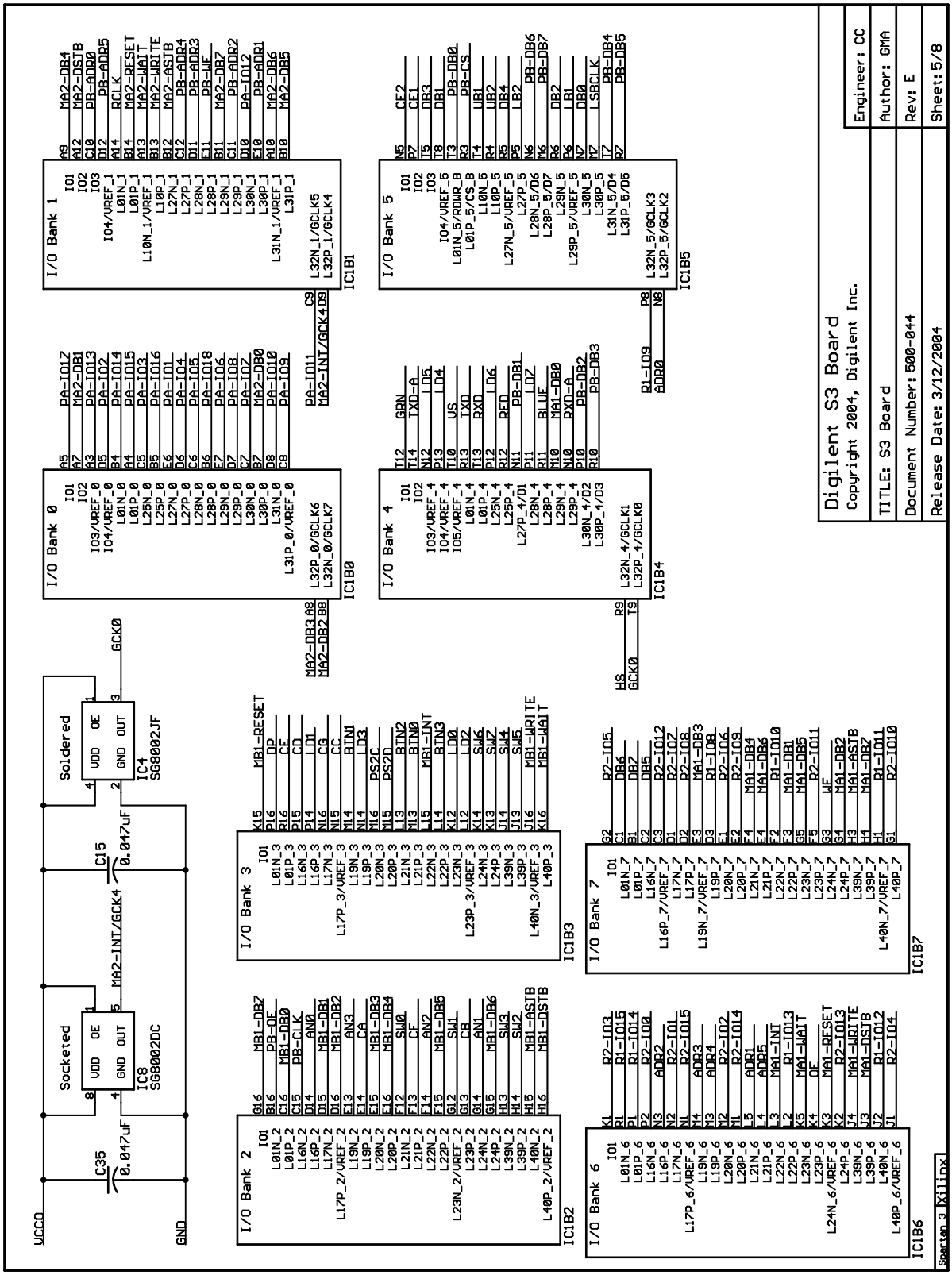
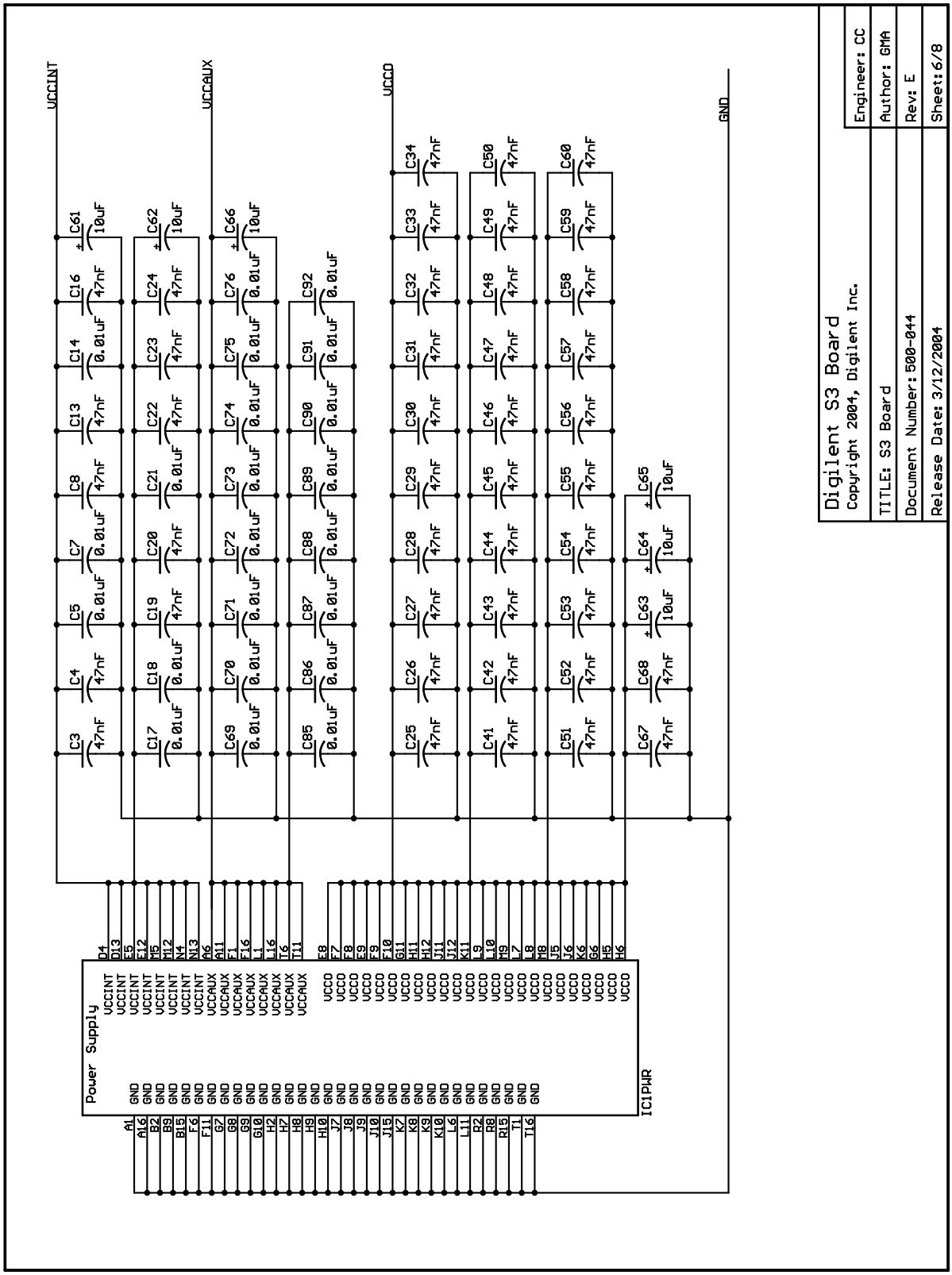



*Figure A-5:* **FPGA I/O Connections, Clock Sources**




UG130_ApA_06_042604

*Figure A-6:* **Power Decoupling Capacitors**

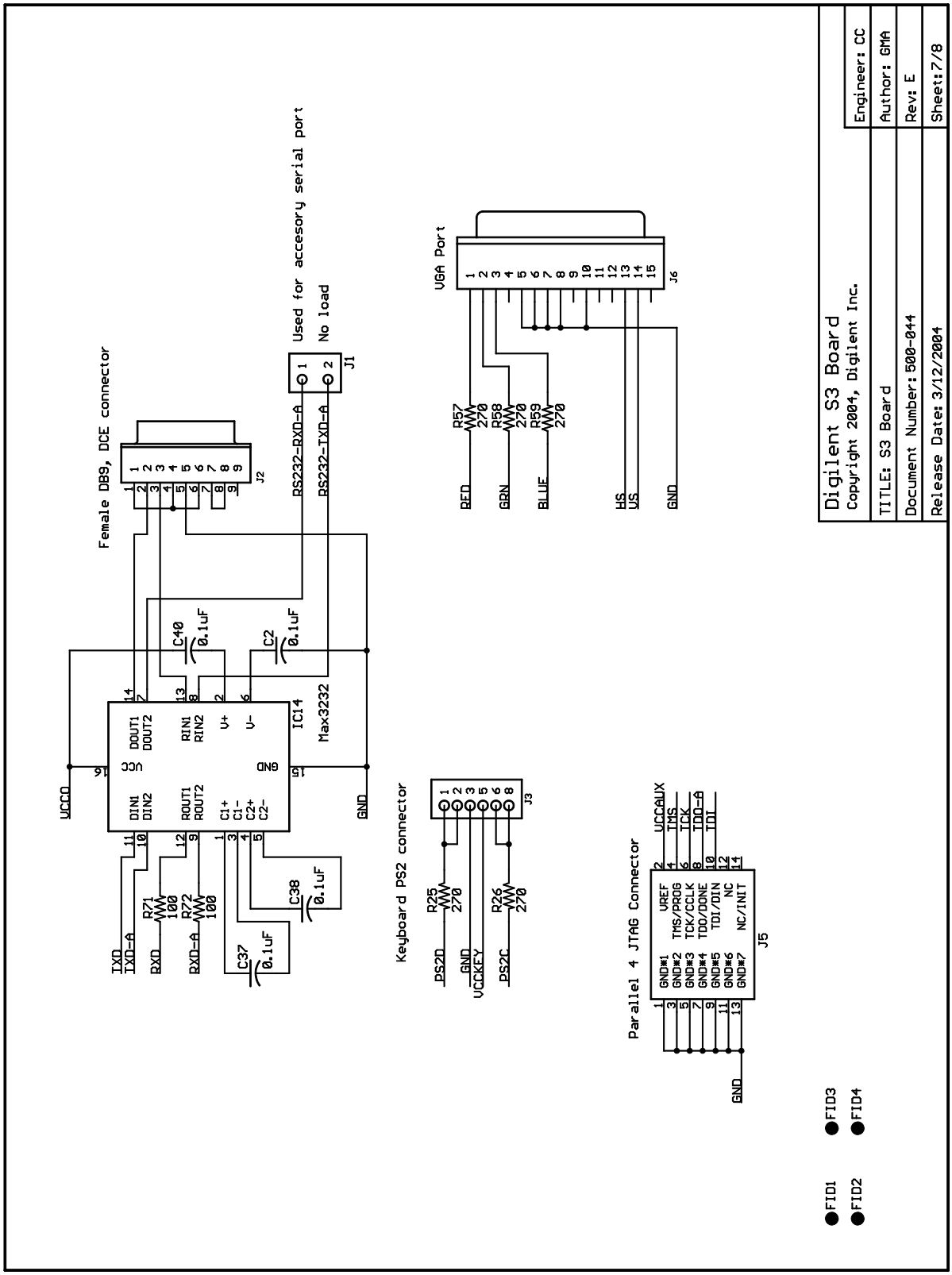



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*Figure A-7:* **RS-232 Serial Port, VGA Port, PS/2 Port, Parallel Cable IV JTAG Interface**

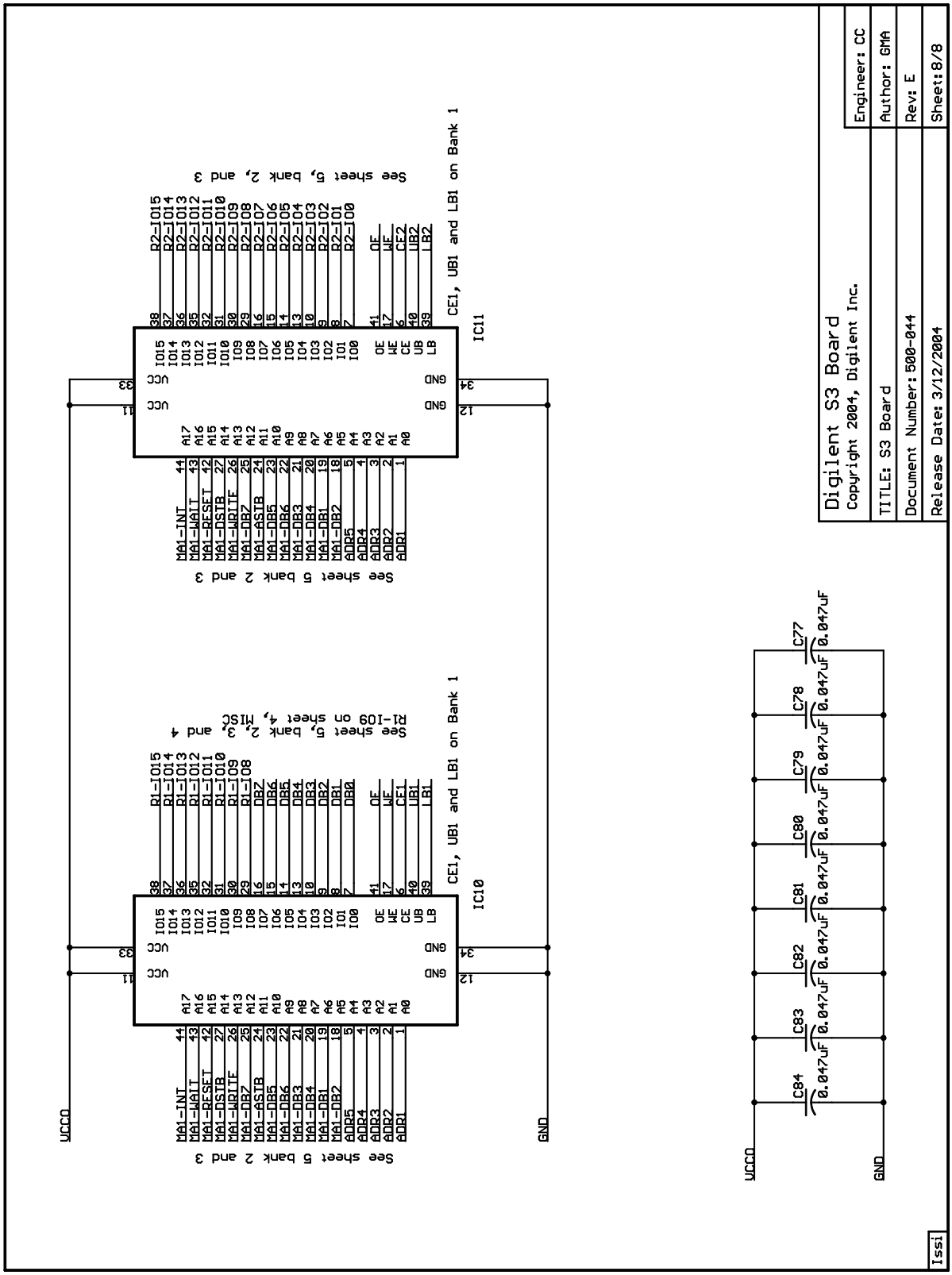


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*Figure A-8:* **2x256Kx16 Fast Asynchronous SRAM Interface**

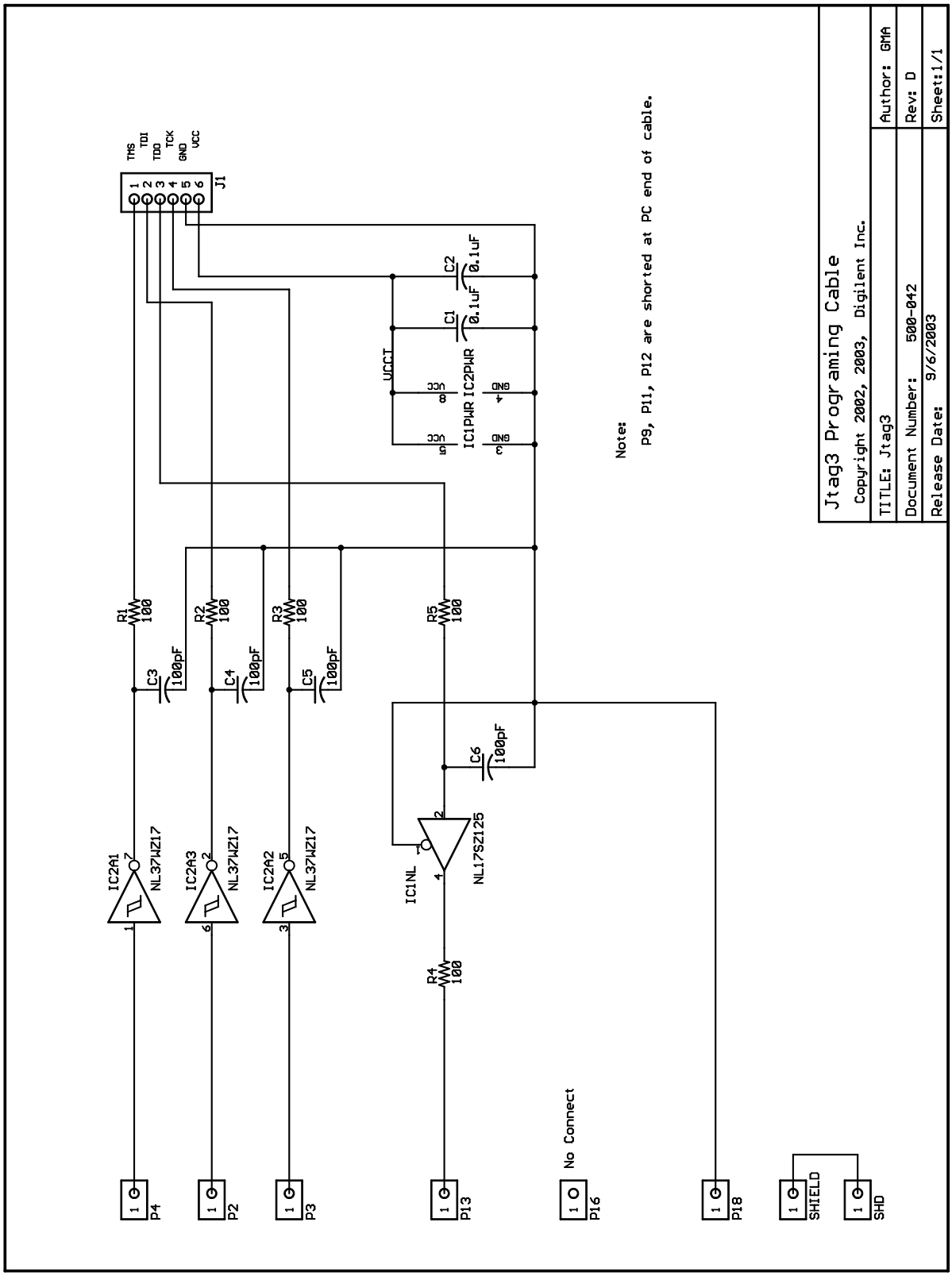


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*Figure A-9:* **Digilent JTAG3 Low-Cost JTAG Download/Debug Cable**

Appendix B

# Reference Material for Major Components

Table B-1 lists the major components on the Spartan-3 Starter Kit Board, including full part numbers and links to complete device data sheets.

*Table B-1:* **Major Components and Data Sheet Links**

| Device | Vendor | Part Number | Description/Data Sheet Link |
|---|---|---|---|
| 1 | Xilinx, Inc. | XC3S200-4FT256C | Spartan-3 FPGA<br>http://www.xilinx.com/bvdocs/publications/ds099.pdf |
| 2 | Xilinx, Inc. | XCF02SVO20C | Platform Flash Configuration Flash PROM<br>http://www.xilinx.com/bvdocs/publications/ds123.pdf |
| 4 | Integrated Silicon Solutions, Inc. (ISSI) | IS61LV25616AL-10T | 256Kx16 Fast Asynchronous SRAM<br>http://www.issi.com/pdf/61LV25616AL.pdf |
| 7 | Maxim | MAX3232 | Dual-Channel RS-232 Voltage Translator<br>http://pdfserv.maxim-ic.com/en/ds/MAX3222-MAX3241.pdf |
| 14 | Epson | SG-8002JF | 50 MHz Crystal Oscillator<br>http://www.knap.at/de/pdf/kat_o/sg8002jf.pdf |
| 25 | Interex | APA-101M-05 | 5V Switching Regulator |
| 27 | National Semiconductor | LM1086CS-ADJ | 3.3V Regulator<br>http://www.national.com/pf/LM/LM1086.html#Datasheet |
| 28 | STMicroelectronics | LF25CDT | 2.5V Regulator<br>http://www.st.com/stonline/books/pdf/docs/2574.pdf |
| 29 | ? | | 1.2V Regulator |